4201A
CLOCK GENERATOR

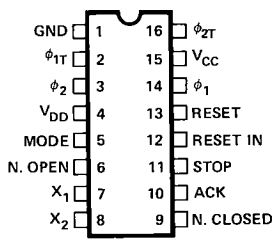
- **Complete Clock Requirements for MCS-40™ Systems**
- **Crystal Controlled Oscillator (XTAL External)**
- **MOS and TTL Level Clock Outputs**
- **Provides MCS-40 Reset Function Signal**
- **Standard Operating Temperature Range of 0° to 70°C**
- **Also Available with -40° to +85°C Operating Range**

The 4201A is a CMOS integrated circuit designed to fill the clock requirements of the MCS-40 microcomputer family. The 4201A contains a crystal controlled oscillator (XTAL external), clock generation circuitry, and both MOS and TTL level clock driver circuits.

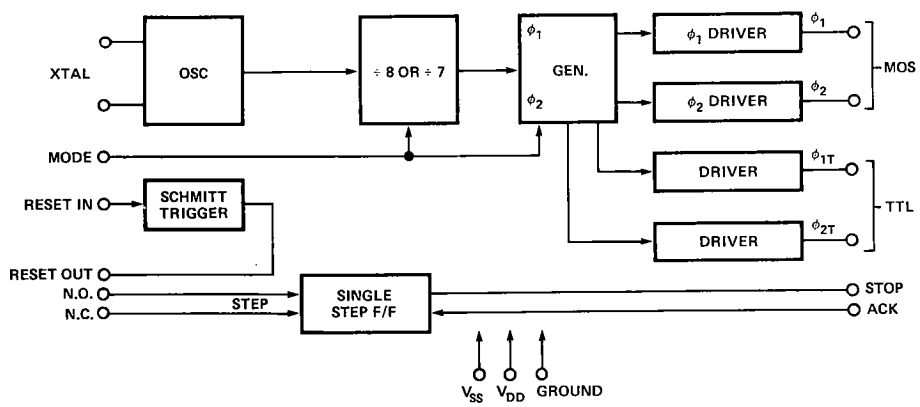
The 4201A also performs the power on reset function required by MCS-40 components and provides the logic necessary to implement the single-step function of the 4040 central processor unit.

PIN CONFIGURATION

4201A



BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Designation	Description of Function
1	GND	Circuit ground potential. This pin can be left floating for low power application. MOS clock output will be operative, TTL clock outputs will not.
2	ϕ_{1T}	Phase 1 TTL level clock output. Positive true.
3	ϕ_2	Phase 2 MOS level clock output. Directly drives all MCS-40 components.
4	V_{DD}	Main Power Supply Pin. $V_{DD} = V_{CC} - 15V \pm 5\%$.
5	MODE	Counter mode control pin. Determines whether counter divides basic frequency by 8 or 7. Mode 1 = $V_{CC} \rightarrow \div 7$ Mode 2 = $V_{DD} \rightarrow \div 8$
6	N. OPEN	Input of single step circuitry to which normally open contact of SPDT switch is connected.
7	X1	External Crystal Connection. This pin may be driven by an external frequency source. X2 should be left unconnected.
8	X2	External Crystal Connection.
9	N. CLOSED	Input of single step circuitry to which normally closed contact of SPDT switch is connected.
10	ACK	Acknowledge input to single step circuitry normally connected to stop acknowledge output of 4040. The ACK input circuitry, contains an internal pull-down resistor, eliminating the need for any external pull-down.
11	STOP	Stop output of single step circuitry normally connected to stop input of 4040. A SPDT toggle switch may be inserted in this line for RUN/HALT control.
12	RESET IN	Input to which RC network is connected to provide power-on reset timing.
13	RESET	Reset signal output which directly connects to all MCS-40 reset inputs. This signal is active low.
14	ϕ_1	Phase 1 MOS level clock output. Directly drives all MCS-40 clock inputs.
15	V_{CC}	Circuit reference potential — most positive supply voltage.
16	ϕ_{2T}	Phase 2 TTL level clock output. Positive true.

FUNCTIONAL DESCRIPTION

The 4201A consists of the following functional blocks:

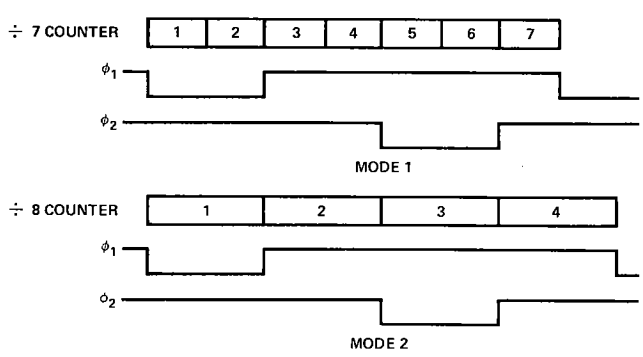
CRYSTAL OSCILLATOR

The oscillator circuit consists of a simple inverter biased in the active region and a crystal phase shift network to provide positive feedback.

PROGRAMMABLE SHIFT REGISTER

The shift register in the 4201A divides the master clock and generates the proper states for generating the desired two-phase clock. The circuit is a seven bit dynamic device which circulates a logical "1" through a field of zeroes. The output of the various states are then combined to provide the proper clock waveforms. This provides a divide by 7 function.

In order to maintain the proper clock timing over the full operating frequency range of the MCS-40™ system, the shift register is programmable (using mode pin) as either a 7 bit or 8-bit device. In the 8-bit mode, the relationship between the phases is equal; that is, ϕ_1 pulse width, ϕ_2 pulse width, ϕ_1 to ϕ_2 and ϕ_2 to ϕ_1 times are all equal.



4201A Shift Register Modes.

PHASE DECODER

A simple gate complex is used to decode the shift register outputs to provide phase 1 and phase 2 clock waveforms. This circuitry is controlled by the mode input to achieve the two sets of timing discussed in the previous section.

OUTPUT BUFFERS

There are two sets of output buffers for the 2 phase clock. One set is the MOS level drivers designed to directly drive a full complement of MSC-40 components. The second set provides TTL compatible outputs which can drive one standard TTL load.

RESET CIRCUIT

The reset circuit is simply a level detector and driver stage. An external RC network connected to the reset input pin of the 4201A as described in the Design Considerations section provides power-on delay. The user's system will determine the required delay.

SINGLE STEP CONTROL

The 4201A contains the necessary circuitry for allowing the 4040 CPU to execute instructions one at a time. Using the stop input and stop acknowledge output of the 4040, the 4201A generates a pulse that allows the 4040 to perform only one instruction. The stop command can be provided by a SPDT pushbutton (break-before-make) directly since debouncing is provided by the 4201A. A SPST toggle switch, in series with the $\overline{\text{STOP}}$ line, provides the Run/Halt feature.

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... -55°C to 150°C Ambient
Operating Temperature ..... 0°C to 70°C Ambient
Maximum Positive Voltage ..... V_{CC} +.5V
Maximum Negative Voltage ..... V_{DD} -.3V
Maximum Power Dissipation 1.0W
Maximum Supply Voltage V_{CC} -V_{DD} ..... 17V[1]
Maximum Supply Voltage V_{CC} -V_{DD} ..... 17V[2]

Notes: 1. C_{LOAD}, ϕ_1 and $\phi_2 \geq 100$pF.
2. C_{LOAD}, ϕ_1 and $\phi_2 = 0$; $R_{DD} = 68\Omega$; Bypass Capacitor at V_{DD} Pin to GND.

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS T_A = 0°C to 70°C; V_{CC}-V_{DD} = 15V ±5%; GND = V_{CC} -5V ±5%.

SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Limit Max.	Units	Conditions
I_{DD}	Supply Current		20	mA	5.185MHz Crystal, C_{LOAD} ϕ_1 and ϕ_2=200pF

INPUT/OUTPUT CHARACTERISTICS

I_{LI}	Input Leakage Current		10	μA	V_{IL} = V_{DD} All inputs except X_1, X_2, N. Open, N. Closed
V_{IH}	Input High Voltage	V_{CC}-1.5	V_{CC}+.5	V	All inputs except X_1, X_2, Reset
V_{IL}	Input Low Voltage	V_{DD}	V_{CC}-13	V	All inputs except X_1, X_2, Reset
V_{OL}	Output Low Voltage	V_{DD}	V_{CC}-13.4	V	Capacitance load only
V_{OH}	Output High Voltage	V_{CC}-1.5	V_{CC}	V	Capacitance load only
V_{OL}	ϕ_{1T}, ϕ_{2T}		GND+.5	V	I_{OL} = 1.6mA
V_{OH}	ϕ_{1T}, ϕ_{2T}	V_{CC}-.75		V	I_{OH} = -400μA
I_{OL}	ϕ_1, ϕ_2 Sink Current	400		mA	V_{OUT} = V_{CC}; Pulse Width ≤1μsec
I_{OL}	ϕ_{1T}, ϕ_{2T} Sink Current	15		mA	V_{OUT} = V_{CC}
I_{OL}	Reset Sink Current	6		mA	V_{OUT} = V_{CC}
I_{OL}	Stop Sink Current	1		mA	V_{OUT} = V_{CC}
I_{OH}	ϕ_1, ϕ_2 Source Current	180		mA	V_{OUT} = V_{DD}
I_{OH}	ϕ_{1T}, ϕ_{2T} Source Current	8		mA	V_{OUT} = V_{DD}
I_{OH}	Reset Source Current	6		mA	V_{OUT} = V_{DD}
I_{OH}	Stop Source Current	1		mA	V_{OUT} = V_{DD}
V_{IL}	Reset Input Low Voltage	V_{DD}	V_{CC}-11	V	
V_{IH}	Reset Input High Voltage	V_{CC}-6.5	V_{CC}+.5	V	
R_1	Pull Up Resistance on N. Open, N. Closed	20	120	KΩ	V_{IN} = V_{DD}

CAPACITANCE f = 1MHz; T_A = 25°C

Symbol	Parameter	Limit Min.	Limit Max.	Units	Conditions
C_{IN}	Input Capacitance		5	pF	All Inputs except X_1, X_2
C_{OUT}	ϕ_1, ϕ_2 Output Capacitance		40	pF	
C_{OUT}	ϕ_{1T}, ϕ_{2T} Output Capacitance		10	pF	
C_{OUT}	Stop Reset Output Capacitance		5	pF	

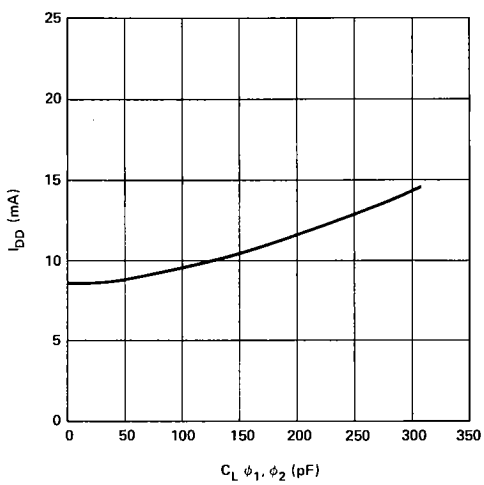
A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$; $V_{CC} - V_{DD} = 15V \pm 5\%$; $G = V_{CC} - 5V \pm 5\%$

Symbol	Parameter	Limit			Units	Conditions
		Min.	Typ.	Max.		
t_{CY}	Clock Period		$t_{XTAL}*7$		ns	Mode = V_{CC}
$t_{\phi PW}$	Clock Pulse Width	$(2/7)t_{CY}-10$	$(2/7)t_{CY}$	$(2/7)t_{CY}+10$	ns	
$t_{\phi D1}$	Clock Delay from ϕ_1 to ϕ_2	$(2/7)t_{CY}-10$	$(2/7)t_{CY}$	$(2/7)t_{CY}+10$	ns	
$t_{\phi D2}$	Clock Delay from ϕ_2 to ϕ_1	$(1/7)t_{CY}-10$	$(1/7)t_{CY}$	$(1/7)t_{CY}+10$	ns	
t_{CY}	Clock Period		$t_{XTAL}*8$		ns	Mode = V_{DD}
$t_{\phi PW}$	Clock Pulse Width	$(1/4)t_{CY}-10$	$(1/4)t_{CY}$	$(1/4)t_{CY}+10$	ns	
$t_{\phi D1}$	Clock Delay from ϕ_1 to ϕ_2	$(1/4)t_{CY}-10$	$(1/4)t_{CY}$	$(1/4)t_{CY}+10$	ns	
$t_{\phi D2}$	Clock Delay from ϕ_2 to ϕ_1	$(1/4)t_{CY}-10$	$(1/4)t_{CY}$	$(1/4)t_{CY}+10$	ns	
$t_{\phi D3}$	TTL Clk to MOS Clk Skew[1]	0		40	ns	
$t_{\phi r}, t_{\phi f}$	Clock Rise and Fall Time			50	ns	C_L=300pF=ϕ_1, ϕ_2; C_L=50pF on ϕ_{1T}, ϕ_{2T}
t_D	Delay from Acknowledge to Stop			1	μs	C_L=20pF

Note: 1. See waveforms section for phase relationships between ϕ_1, $\phi_1 T$, ϕ_2, and $\phi_2 T$.
2. Proper system operation of all members of the MCS-40™ component family is guaranteed with the 4201 Clock Generator at 1.35 μsec $\leq t_{CY} \leq$ 2 μsec.

TYPICAL CHARACTERISTICS

I_{DD} CURRENT VS. LOAD CAPACITANCE



XTAL SPECIFICATIONS

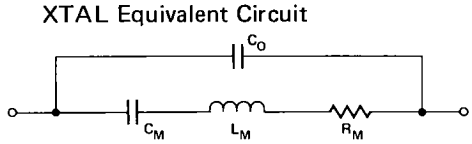
Range: 3.5 - 5.185 MHz

Mode: Series or Parallel Resonant

Recommended: 1. Intel I4801
2. Crystek 5.185 MHz, Spec. No. CY8A
3. CTS Knights MP051

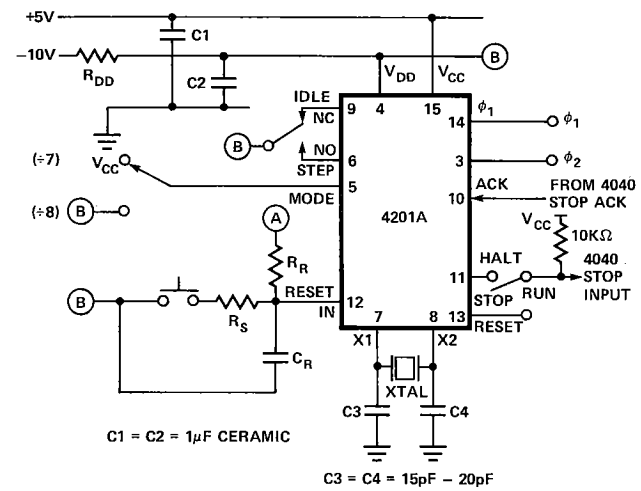
XTAL Capacitance Requirements: 15-20 pF

CTS Knights
XTAL Equivalent Circuit



$C_O \approx$ 3-5pF
$C_M \approx$ 10fF
$R_M \leq 50\Omega$
$L_M \approx \frac{1}{(2\pi f)^2 C_M}$

CLOCK GENERATOR IMPLEMENTATION



DESIGN CONSIDERATIONS

CRYSTALS

Either ÷7 or ÷8 Modes may be used. Mode equals V_{CC} for ÷7, Mode equals V_{DD} for ÷8. The clock frequency range should be between 500 kHz (4 MHz XTAL, ÷8 MODE) and 740 kHz (5.185 MHz XTAL, ÷7 MODE). The crystal may be found as a standard product from Intel distributors, CTS Knights or Crystek.

X1 AND X2 INPUT CAPACITANCE

The XTAL terminals, X1 and X2, should be tied to 15 pF - 20 pF capacitors C3 and C4 to AC system GND.

POWER SUPPLY VOLTAGE CONSIDERATIONS

1. Operation is guaranteed with V_{CC}-V_{DD} = 15V ± 5%. During system power-up or during power supply glitching, the maximum magnitude of (V_{CC}-V_{DD}) must be limited to 17 volts.

   During the power supply rise time (that is, when $|V_{CC}-V_{DD}| < 14.25$ volts), improper ϕ_1, and ϕ_2 output may occur until $|V_{CC}-V_{DD}|$ reaches the 14.25 minimum voltage.

2. With V_{CC} = +5V, V_{DD} = -10V, bypass capacitor C1 of 1 μF and C2 of 1 μF from V_{CC} to GND and V_{DD} to GND, respectively, should provide excellent bypassing. Bypass capacitors should be ceramic or equivalent quality to insure low inductance and low series resistance.

3. The purpose of the current limiting register R_{DD} is both to limit ϕ_1 and ϕ_2 rise times and to drop V_{DD} at the 4201A V_{DD} pin. Values for R_{DD} as a function of ϕ_1, ϕ_2 load capacitance are:
   For C_{LOAD} <50 pF; use R_{DD} = 100Ω.
   For 50 pF <C_{LOAD} <100 pF; use R_{DD} = 68Ω.
   For 100 pF <C_{LOAD} <300 pF; use R_{DD} = 27Ω.
   For C_{LOAD} >300 pF; use R_{DD} = 10Ω.

   All 4201A functions requiring the V_{DD} voltage should use the pin V_{DD} or node (B) on the 4201A side of resistor R_{DD}. Operation with the voltage drop across R_{DD} is guaranteed by Intel testing.

4. Single-Supply System (+15 V or -15)

   Recommended 4201A circuit modifications for single supply systems are:

   1. The 1 μF ceramic capacitor C1 should be between 4201A V_{DD} and V_{CC} pins.
   2. Other capacitors shown as being grounded should be connected to V_{CC}.
   3. Reset R_R is connected to V_{CC}. Reset C_R is connected to V_{DD} pin.
   4. The current limiting resistor R_{DD} is still needed in the V_{DD} line.

5. Power Supply Rise Times

   Intel testing is for power supply rise times between 5 ms and 300 ms. For power supply rise times less than 5 ms, a 200KΩ resistor from X1 to GND and C3 = C4 = 5 pF is recommended.

RESET NETWORK

The Reset input has V_{IL} = V_{CC}-11 volts and V_{IH} = V_{CC} -6.5 volts, with about 1 volt of hysteresis (Schmitt circuit).

Node (A) must be tied to GND or V_{CC} = +5 V; and R_R and C_R selected, such that the negative V_{DD} transition moves the Reset input below V_{IL}.

Tying node (A) to GND and making C_R very large, i.e. >1μF, will allow the greatest freedom in V_{CC} and V_{DD} rise times during turn-on. Tying node (A) to GND will also cause Reset after a V_{DD} glitch to GND.

The purpose of R_S at 510Ω or 1KΩ is to limit Reset input fall time on manual Reset, so that the Reset input does not fall below V_{DD}.

TTL CLOCK OUTPUTS

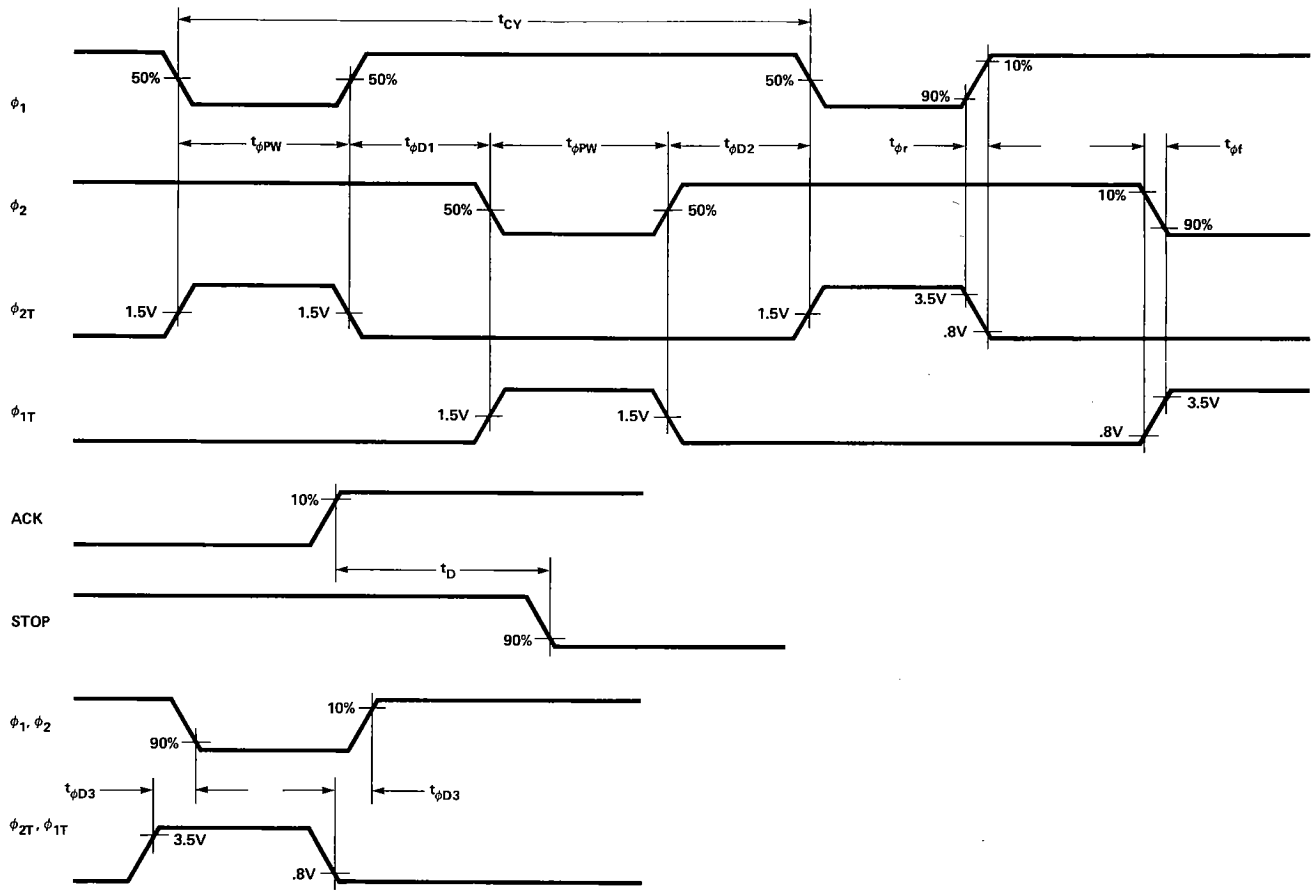
If ϕ_{1T} and ϕ_{2T} are used, GND pin should be tied to logic ground. ϕ_{2T} levels will swing between V_{CC} and GND.

UNUSED FUNCTIONS

If any of the 4201A functions listed below are not used, for power conservation it is recommended that the pins be connected as described below:

1. ϕ_{1T},ϕ_{2T}
   Tie GND pin, ϕ_{1T}, ϕ_{2T} to V_{CC}.
2. Single step
   Tie NO to V_{CC}.
   Tie NC to Node (B) (V_{DD} pin).
   Tie STOP ACK to V_{CC}.
   STOP left open.
3. Reset
   Tie RESET IN, RESET OUT to V_{CC}.

WAVEFORMS



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Printed in U.S.A./A-53/1076/1K