intel®

4265
PROGRAMMABLE GENERAL PURPOSE I/O DEVICE

- Multi-Mode 14 Operating Modes
- 16 Lines of I/O Capability
- Bit Set/Reset
- Multiplexable Outputs
- Eight Bit Transfer Mode
- Interfaces to 8080 Peripherals
- Synchronous and Asynchronous Interface
- Strobed Buffer Inputs and Outputs
- TTL Interface
- Up to Eight 4265s Per System
- Interface to Standard RAMs
- 28 Pin Dual-In-Line Package
- Interface to Standard RAMs
- 28 Pin Dual-In-Line Package
- Standard Operating Temperature Range of 0° to 70°C
- Also Available with -40° to +85°C Operating Range

The 4265 is a general purpose I/O device designed to interface with the MCS-40™ microcomputer family. This device provides four software programmable 4-bit I/O ports which can be configured to allow any one of fourteen unique operating modes for interfacing to data memory or a variety of user peripheral devices.

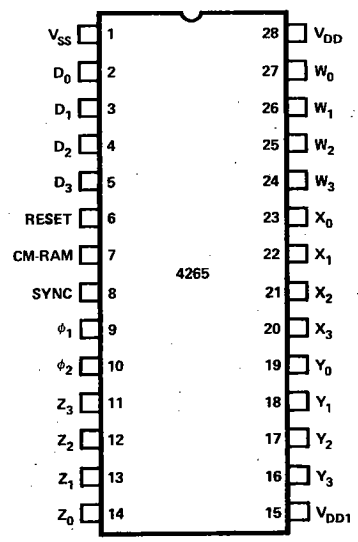
A single MCS-40 system can accomodate up to four 4265s (one per CM-RAM) without external logic or up to eight 4265s with one external decoder.

The 4265 resides on the MCS-40 data bus and uses the same selection procedure as 4002 RAM device. A valid compare selects the 4265 for MCS-40 I/O commands. As in the case of the 4002 or any MCS-40 peripheral circuit, selection occurs only when the proper SRC code and the CM signal are present simultaneously.

The 4265 provides an extremely flexible, general purpose I/O system capable of handling 4- or 8-bit input or output data. One of fourteen basic operating modes can be selected (software programmable) as described below.

Port Z is TTL compatible with any TTL device. Ports W, X, and Y are low-power TTL compatible.

PIN CONFIGURATION

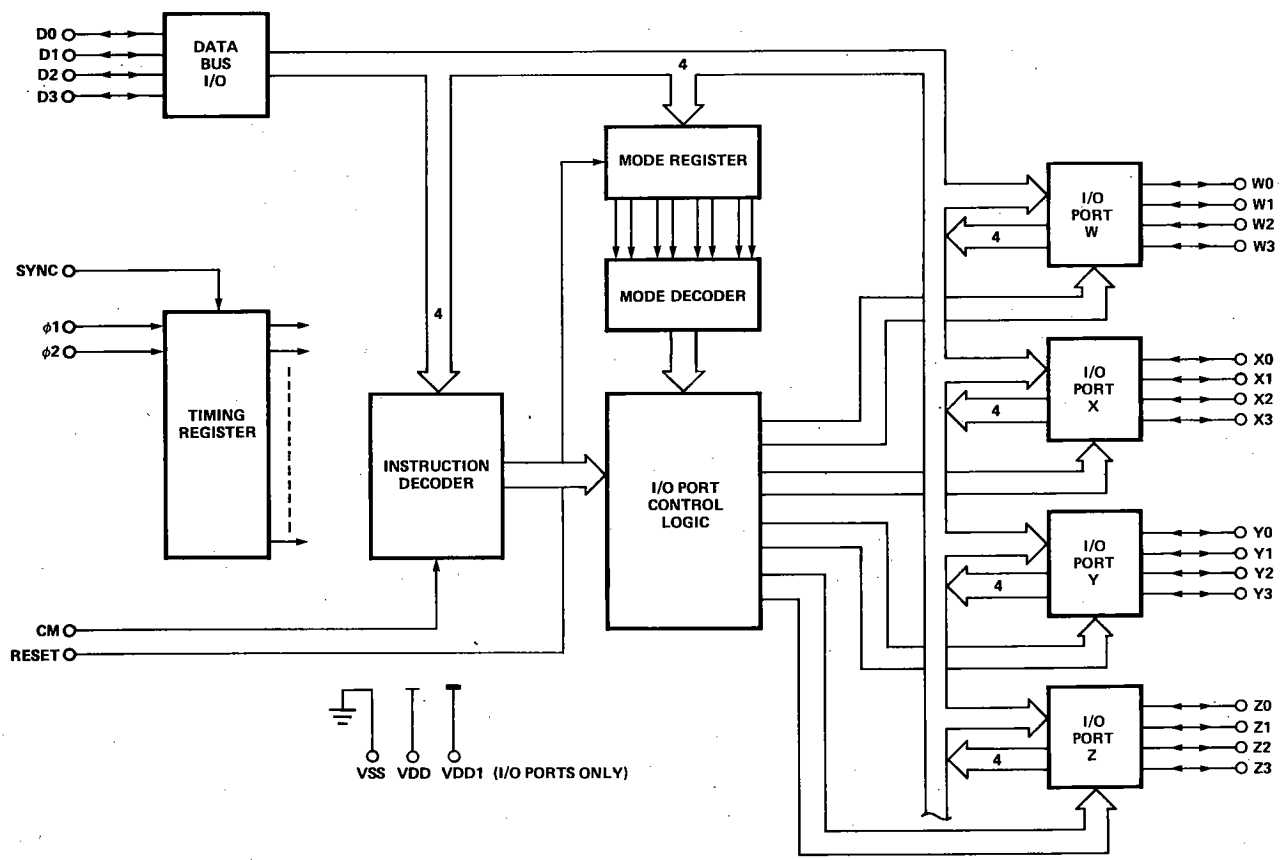


JULY 1976

Pin Description

Pin No.	Designation	Function
2-5	D0-D3	Bi-directional data bus. All address, instruction and data communication between processor and I/O ports are transferred on this port.
6	RESET	A negative level (V_{DD}) applied to this pin clears all storage elements, places the 4265 in the Reset Mode and deselects the device.
7	CM	Command input driven by a CM-RAM output of the processor. Used for decoding SRC, RDM, WRM,WMP,SBM, ADM, WR0-3 and RD0-3.
9-10	ϕ1-ϕ2	Non-overlapping clock signals which determine timing.
8	SYNC	Synchronization signal generated by the processor; indicates the beginning of an instruction.
24-27 20-23 16-19 11-14	W3-W0 X3-X0 Y3-Y0 Z3-Z0	Four programmable I/O ports having different functional designation depending on 4265 mode of operation. A data bus "1" negative true (V_{DD}) will appear on a port as a "1" positive true (V_{SS}). These ports are TTL compatible.
28	V_{DD}	Main power supply pin. Value must be V_{SS} -15V ±5%.
15	V_{DD1}	Supply voltage for I/O ports.
1	V_{SS}	Most positive supply voltage (V_{DD1} = 0V, V_{SS} = 5V for TTL I/O ports. V_{DD1} = V_{DD} for MOS loads only).
28 = TOTAL PINS		

4265 HARDWARE BLOCK DIAGRAM



4265 PROGRAMMABLE MODES

OPERATING MODES

- Mode 1 — 8-Bit Asynchronous I/O Port (Bidirectional)
  4-Bit Input Port (Unbuffered)
- Mode 2 — 8-Bit Asynchronous I/O Port (Bidirectional)
  4-Bit Output Port
- Mode 3 — 8-Bit Synchronous I/O Port (Bidirectional)
  4-Bit Synchronous Output Port
- Mode 4 — Four 4-Bit Output Ports
- Mode 5 — Three 4-Bit Output Ports
  One 4-Bit Input Port (Unbuffered)
- Mode 6 — Two 4-Bit Output Ports
  Two 4-Bit Input Ports (Unbuffered)
- Mode 7 — One 4-Bit Output Port
  Three 4-Bit Input Ports (Unbuffered)
- Mode 8 — Three 4-Bit Synchronous Output Ports
- Mode 9 — Two 4-Bit Synchronous Output Ports
  One 4-Bit Asynchronous Input Port

OPERATING MODES

- Mode 10 — One 4-Bit Synchronous Output Port
  Two 4-Bit Asynchronous Input Ports
- Mode 11 — Three 4-Bit Asynchronous Input Ports
- Mode 12 — 8-Bit Address Port
  4-Bit Synchronous I/O Port (Bidirectional)
  2 Device Selection Control Signals
- Mode 13 — 8-Bit Address Port
  4-Bit Asynchronous I/O Port (Bidirectional)

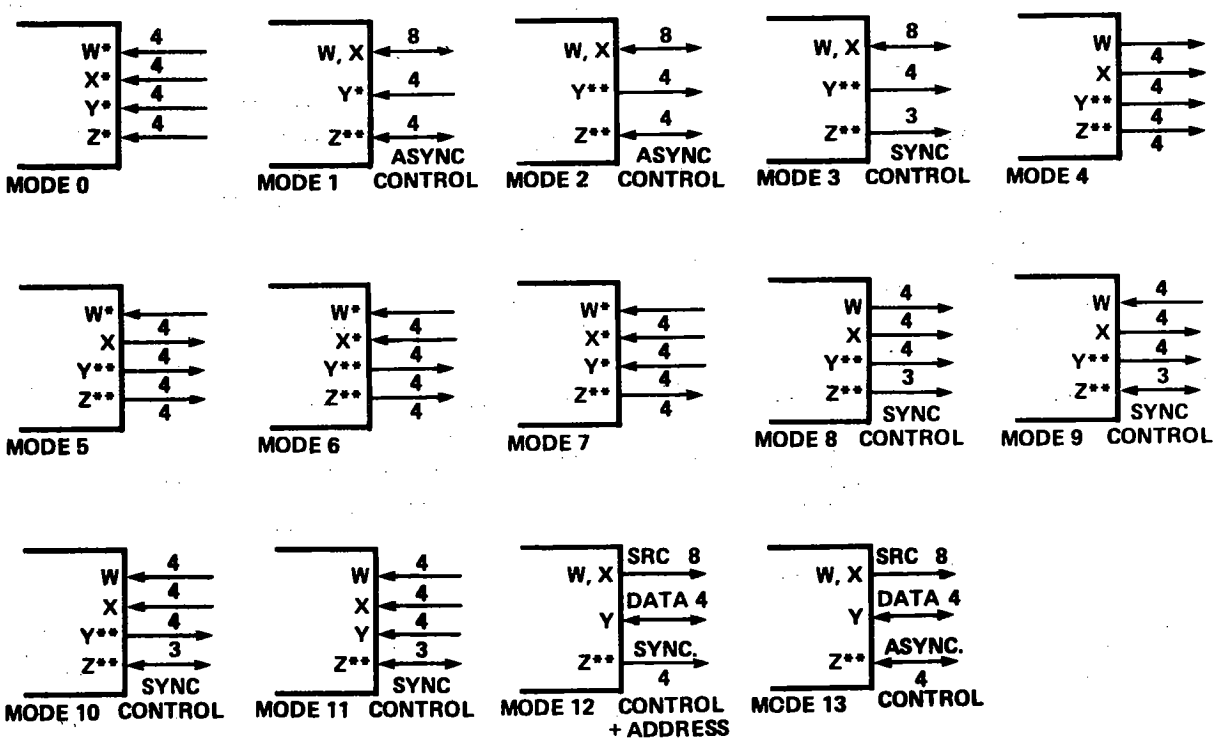
CONTROL AND OPERATING MODE

- Mode 0 — Four 4-Bit Input Ports (Unbuffered)
  Resets I/O Buffers

CONTROL MODES

- Mode 14 — Disables all output buffers, allowing another 4265 to be multiplexed at the port level.
- Mode 15 — Enables output buffers, previous mode restored.

4265 MODE DIAGRAM



* UNBUFFERED INPUT PORTS.

**THE LINES ON THESE PORTS ARE SUBJECT TO THE BIT SET COMMAND.

Functional Description

Control Functions: Two types of operations are possible with the 4265. The device (once selected) can be programmed to one of fourteen basic operating modes. This is accomplished by executing a WMP instruction which sends the 4-bit content of the CPU's Accumulator to the 4265 where it is decoded and used to logically configure the device. A second Control operation makes use of the WRM instruction to select one of eight output lines (Port Y or Z) and perform a SET or RESET operation on that line. This is accomplished by interpreting the 4-bit Accumulator value as follows: The upper three bits select one of eight output latches; the least significant bit determines whether a SET or RESET operation is to be performed.

Data Transfer Functions: The remaining eleven instructions provide four WRITE operations (WR0, WR1, WR2, WR3) and seven READ operations (RD0, RD1, RD2, RD3, ADM, SBM, RDM). These allow data in 4-bit or 8-bit format to be transmitted between the 4265 and external I/O devices or memory devices (all transfers between processor and 4265 are 4-bit transfers).

The sixteen lines of the 4265 are grouped into four ports, four bits each referred to as W, X, Y and Z. The ports can be interrogated by a RD0-3 corresponding to ports W - Z respectively. This means that even when a port is designated as a control port or an output port, the state of the port can be inputted by a RD0-3 instruction (except in modes 12 and 13). The WR0-3 instruction will load the ports W - Z designated outputs. When a port is specifically designated as an input port, it will not respond to an output type instruction (WR0-3, WRM, etc.). See specific mode selection for details.

When port Y or Z is designated an output, regardless of the mode, then it will respond to the Bit Set command. The Bit Set Command allows the user to set the polarity of a single bit without affecting any other bit. This is particularly useful when the output port of interest drives control lines tied to the user system. The user can selectively alter the bit polarity. To alter a bit, the MCS-40 WRM command is utilized.

The 4265 is selected via the CM-RAM line and an appropriate MCS-40™ SRC command. The upper two bits of data at X2 of an SRC instruction with the CM-RAM signal are compared with an address code internal to the 4265. One standard code is available, a code of 2. This allows one 4265 per CM-RAM or up to four per system without additional logic. By using one external decoder and the ability of the DCL (Designate Command Line) instruction to code the CM-RAM lines, up to eight 4265s can be used in a system. Other peripheral devices can share a CM-RAM line with the 4265 (except Mode 12 and 13). For example, a CM-RAM line can contain three 4002 RAMs and one 4265.

The operating modes of the 4265 are selected under program control by the processor. When a 4265 is designed into a specific application, one functional mode is selected. With the possible exception of RESET, ENABLE, and DISABLE, a functional change in mode would not normally be initiated by the software once the part is designed into a specific application. Since mode selection is done with software, the system's "power up" software routine should sequentially establish the mode of each 4265 prior to "main body" program initiation. The mode selection is accomplished with the accumulator operand of the WMP command.

MODE DEFINITION AND TIMING

Detailed Description of Operating Modes

Table 1 provides a listing of the basic operating modes and the appropriate port configuration as determined by the Accumulator value sent to the 4265 during execution of the WMP instruction. A description of each mode is found in the following sections.

Table 1. Detailed Description of 4265 Operating Modes.

Mode	Port W	Port X	Port Y	Port Z			
0	Input port, unbuffered	Input port, unbuffered	Input port, unbuffered	Input port, unbuffered			
1	Bi-directional; Outputs enabled by signal Z0; When enabled output assumes value loaded by WR0.	Bi-directional; Outputs enabled by signal Z0; When enabled output assumes value loaded by WR1.	Unbuffered input port	Bit 0 Asynchronous input used to enable data out on Ports W, X.	Bit 1 Asynchronous input used to load data to Port W, X input buffers.	Bit 2 Output signal which is normally at V_{SS}. Goes to V_{DD1} on execution of WR 1. Returns to V_{SS} on trailing edge of Z0.	Bit 3 Output signal which is normally at V_{SS}. Goes to V_{DD1} on trailing edge of Z1 and remains at V_{DD1} until execution of RD1.
2	Bi-directional; Output enabled by signal Z0; When enabled output assumes value loaded by WR0.	Bi-directional; Outputs enabled by signal Z0; When enabled output assumes value loaded by WR1.	Buffered output port				
3	Bi-directional; Outputs enabled during WR1 cycle. Output assumes value loaded by WR0.	Bi-directional; Outputs enabled during WR1 cycle. Output assumes value loaded by WR1.	Buffered output port	Synchronous output. Normally at V_{SS}; goes to V_{DD1} during execution of WR 1.	Synchronous output. Normally at V_{SS}; goes to V_{DD1} during RD1 instructions.	Synchronous output. Normally at V_{SS}; goes to V_{DD1} during WR2 instructions.	Unassigned. Line is an output and can be set with WRM. Normally at V_{SS} after mode 3 set.
4	Buffered output port	Buffered output port	Buffered output port	Buffered output port			
5	Unbuffered input port	Buffered output port	Buffered output port	Buffered output port			
6	Unbuffered input port	Unbuffered input port	Buffered output port	Buffered output port			
7	Unbuffered input port	Unbuffered input port	Unbuffered input port	Buffered output port			
8	Buffered output port	Buffered output port	Buffered output port	Output signal normally at V_{SS}; goes to V_{DD1} during WR0.	Output signal normally at V_{SS}; goes to V_{DD1} during WR 1.	Output signal normally at V_{SS}; goes to V_{DD1} during WR2.	Unassigned output. Normally at V_{SS} after mode 8 set.
9	Buffered input port, loaded by signal Z0.	Buffered output port	Buffered output port	Input signal used to load Port W asynchronously.	Output signal normally at V_{SS}; goes to V_{DD1} during WR1.	Output signal normally at V_{SS}; goes to V_{DD1} during WR2.	Unassigned output. Normally at V_{SS} after mode 9 set.
10	Buffered input port, loaded by signal Z0.	Buffered input port, loaded by signal Z1.	Buffered output port	Input signal used to load Port W asynchronously.	Input signal used load Port X asynchronously.	Output signal normally at V_{SS}; goes to V_{DD1} during WR2.	Unassigned output. Normally at V_{SS} after mode 10 set.
11	Buffered input port, loaded by signal Z0.	Buffered input port, loaded by signal Z1.	Buffered input port, loaded by signal Z2.	Input signal used to load Port W asynchronously.	Input signal used to load Port X asynchronously.	Input signal used to load Port Y asynchronously.	Unassigned output. Normally at V_{SS} after mode 11 set.
12	Buffered output port, loaded by SRC instructions—contains upper 4-bits of SRC data.	Buffered output port, loaded by SRC instructions—contains lower 4-bits of SRC data.	Bi-directional; Outputs enabled at any WR instruction; input port unbuffered.	Output signal normally at V_{SS}; goes to V_{DD1} during any WR instruction.	Output signal normally at V_{SS}; goes to V_{DD1} during any RD instruction.	Output signal which is loaded with address bit corresponding to WR or RD operation.	Output signal which is loaded with address bit corresponding to WR or RD operation.
13	Buffered output port, loaded by SRC instructions—contains upper 4-bits of SRC data.	Buffered output port, loaded by SRC instructions—contains lower 4-bits of SRC data.	Bi-directional; Outputs enabled by signal Z0; Inputs loaded by signal Z1.	Asynchronous input used to enable data out on Port Y.	Asynchronous input used to load data to Port Y input buffers.	Output signal normally at V_{SS}; goes to V_{DD1} on execution of WR instruction. Returns to V_{SS} on trailing edge of Z0.	Output signal normally at V_{SS}; goes to V_{DD1} on trailing edge of Z1 and remains at V_{DD1} until execution of RD instruction.
14	All outputs disabled, data saved.	All outputs disabled, data saved.	All outputs disabled, data saved.	All outputs disabled, data saved.	All outputs disabled, data saved.	All outputs disabled, data saved.	All outputs disabled, data saved.
15	Previous information restored.	Previous information restored.	Previous information restored.	Previous information restored.	Previous information restored.	Previous information restored.	Previous information restored.

a. Reset Mode – Mode 0

WMP Operand – 0000

Mode Description: The Reset Mode provides for a programmable reset. Reset will clear all I/O buffers; however, reset will not clear the chip select flip-flop. Hence, the 4265 will remain selected and enabled after a programmable reset. A negative 1 level (V_{DD}) on the RESET pin will cause a response similar to the Reset Mode. The only difference is that the 4265 will be enabled but deselected.

Port Description: Ports W, X, Y, and Z are unbuffered input. Hence, they can be read with RD0-3, transferring the state of the port lines into the accumulator. A positive "1" (V_{SS}) will appear in the accumulator as a negative true "1" (V_{DD}). Port Y will also respond to the RDM, SBM and ADM instructions.

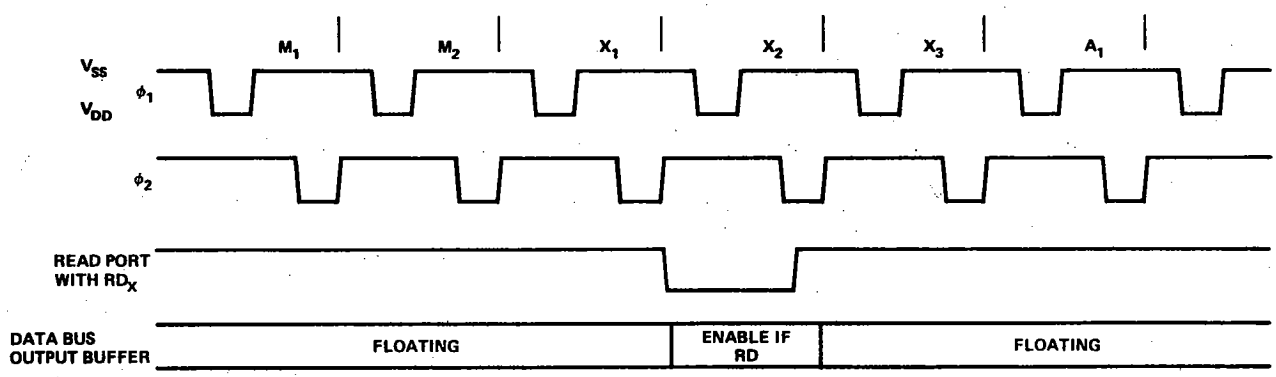
b. 8-Bit Asynchronous I/O Mode with Input – Mode 1

WMP Operand – 0001

Mode Description: The 8-bit I/O mode is used to transfer bi-directional data bytes between the MCS-40™ and the peripheral circuits. Four control lines (Port Z) allow an asynchronous information transfer. Two signals are associated with the input function and two with the output function. Port Y is defined as an unbuffered input.

Port Description

Port W, X		These two ports are combined to transfer 8-bits of I/O under asynchronous control of Port Z. Port W will be loaded with a WR0 and Port X will be loaded with WR1. The WR1 will initiate the write "handshake" on Port Z. When the two ports are interrogated, a sequential RD0 and RD1 will cause the IA line to be deactivated.
Port Y		This port is an unbuffered input, interrogated with an RD2, RDM, ADM or SBM instruction.
Port Z		
Z0	OA	Output acknowledge to the 4265 from the users logic. This signal is activated by the users logic (made negative) in response to the OI signal. The OA signal will enable the 4265 output buffer onto Ports W and X. It should be sufficiently long to allow the transfer.
Z2	OI	Output initiate from the 4265. This signal will be generated when Port X has been loaded via a WR1. Port W and Port X should be loaded in the WR0-WR1 sequence. When the OI signal is active, the external device will request data with the OA. The trailing edge of OA will cause the 4265 to remove the OI. If no OA response is received, OI will be active until the next WR0, where it will be removed until the next WR1.



265 Mode 0 Timing.

Z1	II	Input initiate to the 4265 from the users logic. The signal will be used as a strobe signal to latch the 8-bit contents of the Port W, X lines into the respective buffers. Data is transferred on the negative to the positive transition. This transition will cause the IA signal to be set.
Z3	IA	Output from the 4265. The IA signal will transition to the positive state when an RD1 command is executed. This indicates that the processor has interrogated Port W, X buffer. The processor should read the data in the sequence of RD0 followed by an RD1.

c. 8-Bit Asynchronous I/O Mode with Output – Mode 2

WMP Operand – 0010

Mode Description: Same as for Mode 1, except Port Y is a buffered output port.

Port Description: Port W, X, Z; same as for Mode 1. Port Y: This port is a buffered output port which can be loaded with a WR2 instruction and can be read by an RD2, RDM, ADM, and SBM.

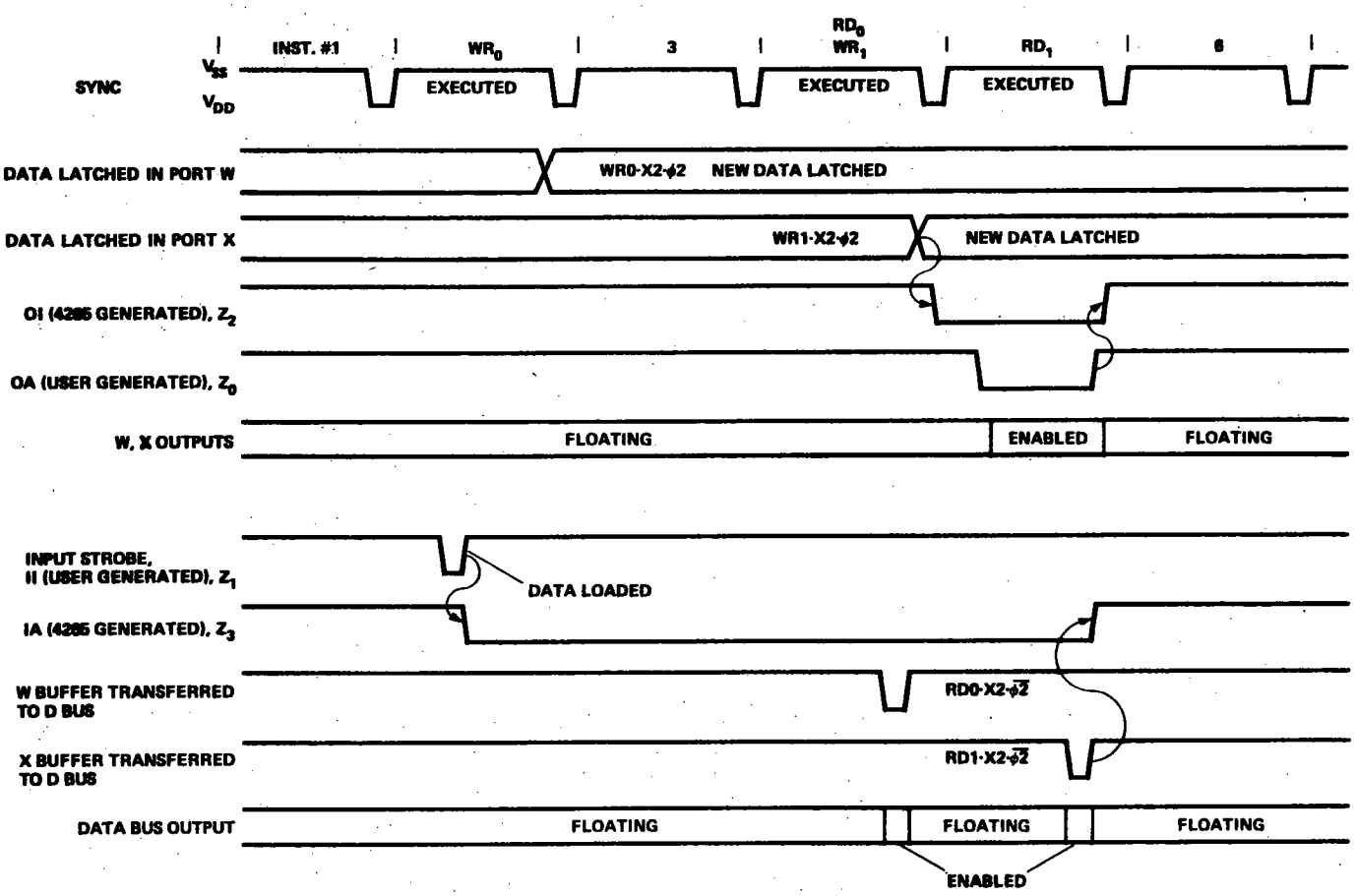


Figure 2. 4265 Modes 1 and 2 Timing.

d. 8-Bit Synchronous I/O Mode with Output – Mode 3

WMP Operand – 0011

Mode Description: This mode is functionally similar to Modes 1 and 2 in terms of its byte transfer feature. However, the transfer control is synchronous. Port W, X are buffered outputs or unbuffered inputs, depending on the direction of transfer. Port Z provides the synchronous strobe control. Port Y is a buffered output port.

Port Description

Port W, X — These two ports are combined to transfer bi-directional 8-bit information under synchronous control. Output data should be loaded into Ports W, X with the WR0-WR1 sequence. The input of information should be sequentially read with an RD0 followed by an RD1.

Port Y — This port is a 4-bit output port. Information is valid during the output strobe of a WR2 command. The output strobe is the Z2 line of the Z port. This port may also be read with an RD2, RDM, ADM and SBM.

Port Z

Z0	OS	Output strobe from 4265. This line is valid during a WR1 command. Information from the output buffers of Ports W and X is present at Ports W and X output lines only during the signal.
Z1	IS	Input strobe from 4265. This line is valid during an RD0 command. Information is taken off the Port W, X lines and is latched in the Port W, X buffers. The RD0 will read the information pertaining to Port W. RD1 will input information pertaining to Port X. The ports must be read by RD0 followed by an RD1. Data will be latched in the W and X Ports with the RD0. Information should be valid at the trailing edge of IS.
Z2	YS	Port Y output strobe from the 4265. This line is valid during a WR2 command. Information will be valid at the Port Y output buffer during this strobe.
Z3		This line is not used. It can be bit set/reset under program control.

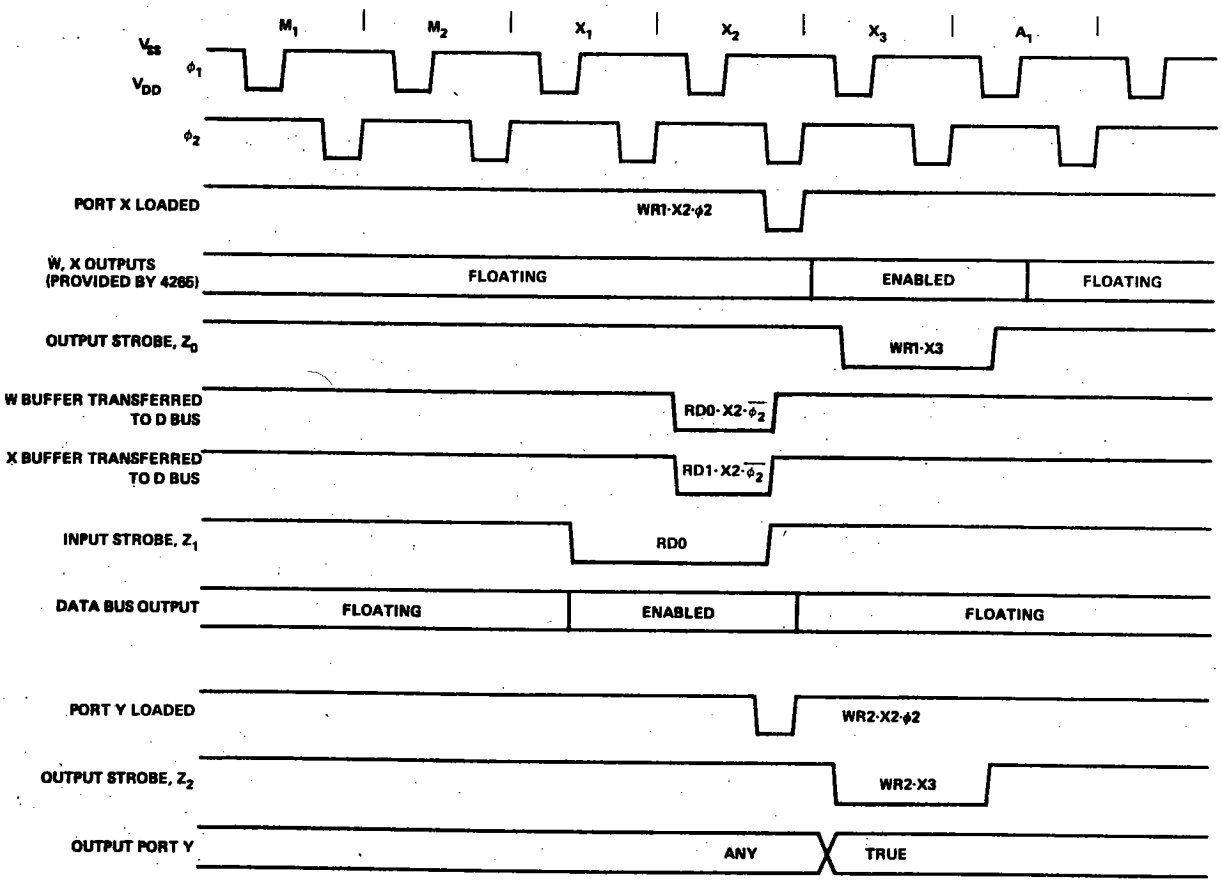


Figure 3. 4265 Mode 3 Timing.

e. Four Port Programmable I/O Modes – Modes 4-7

WMP Operand – 0100-0111

Mode Description: These modes consist of four combinations of static buffered outputs and unbuffered inputs. When combined with the Reset Mode, all combinations of inputs and outputs on four ports are possible.

Port Description: The following five modes have static buffered outputs (0) or unbuffered inputs (I).

WMP	Port:	W	X	Y	Z
0100		0	0	0	0
0101		I	0	0	0
0110		I	I	0	0
0111		I	I	I	0
0000 (reset mode)		I	I	I	I

Those ports of Y and Z designated outputs are subject to bit set/reset capability. All output buffers may be read with the respective RDx (RD0-RD3). Port Y will respond to RDM, ADM and SBM in addition to RD2.

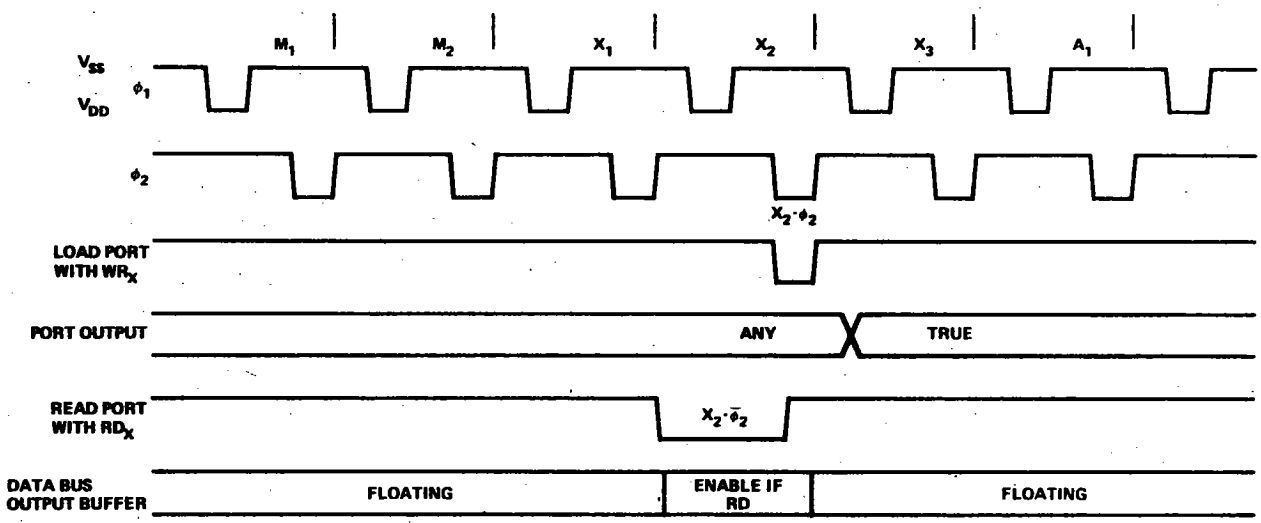


Figure 4. 4265 Modes 4-7 Timing.

f. Three Port Programmable I/O Mode with Synchronous Output and Asynchronous Input Port – Modes 8-11

WMP Operand – 1000-1011

Mode Description: Each 4-bit port can be configured as a buffered input or buffered output port and each has its own control line for synchronizing data transfers. As an example, if in Mode 8, when the processor executes a WR0 instruction, 4-bits of data are transferred to the Port W output buffer and subsequently to the Port W output lines. Output Strobe Z0 serves as a data valid signal which can be used by external logic to latch the data. In Mode 11, Input Strobe Z0 is used to latch the 4-bit data appearing on the Port W lines into the Port W input buffer. The Input Strobe is user generated.

Port Description: The following five modes have synchronous outputs (0) or asynchronous inputs (1):

WMP	Port:	W	X	Y	Z0	Z1	Z2	Z3
1000		0	0	0	W	W	W	X
1001		I	0	0	R	W	W	X
1010		I	I	0	R	R	W	X
1011		I	I	I	R	R	R	X

Where: R = input strobe independent of instruction executed
W = output strobe (WR0-2) from 4265
X = not used

Port Y will respond to RDM, SBM and ADM in the same way as an RD2. Z3 is unused and may be bit set/reset. All output buffers may also be read with the respective RDx.

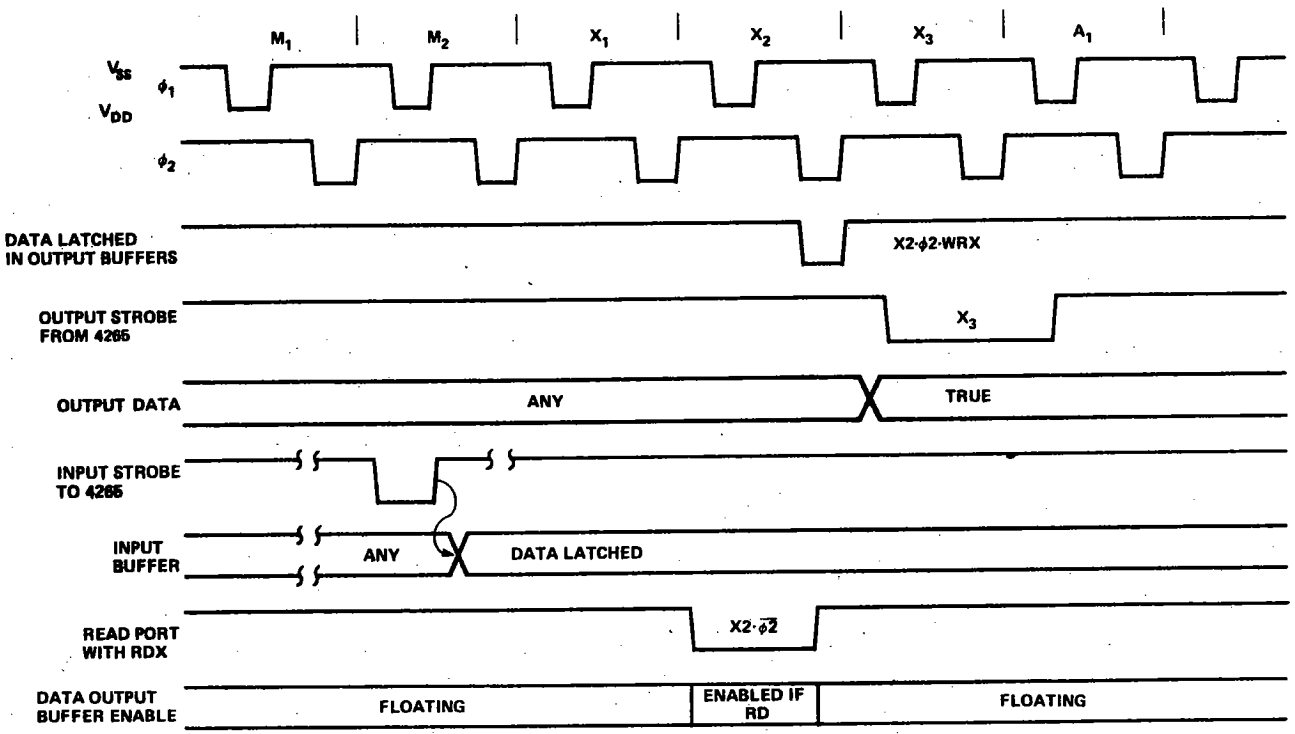


Figure 5. 4265 Modes 8-11 Timing.

g. 4-Bit I/O with 8-Bit SRC Address and 4-Bit Synchronous Control Port – Mode 12

WMP Operand – 1100

Mode Description: In this mode, the most recent 8-bit SRC operand is displayed on Port W and X. The 4265 will treat all SRC instructions as being valid as long as the CM-RAM line for this 4265 has been selected by an appropriate DCL (Designate Command Line) instruction. Ports W and X will change each time they receive an SRC and CM-RAM. The 4-bit data port (Port Y) will perform bi-directional synchronous I/O. The port output buffer may be loaded with a WR0-3 and the port input buffer will be read with RD0-RD3, RDM, SBM or ADM. The control port will provide mutually exclusive input or output strobes depending on the current instruction. Two of the control lines may be used for device selection. This mode can be used to interface up to 1K of external storage (RAM-2111, 4101, 5101) or a multitude of external I/O devices. Once this mode is programmed, all SRC values will not be treated as 4265 selection or deselection instructions.

Port Description

Port W, X	This port will display the most recent SRC and will be altered with each SRC when selected. Otherwise, the output is static.
Port Y	This is a bi-directional data port that will latch data with a RD0-RD3, RDM, ADM, and SBM. The port will output data with a WR0-WR3.

Port Z

Z0	OS	Output strobe from 4265. Active during WR0-WR3. Data will be valid during this strobe.
Z1	IS	Input strobe from 4265. Active during RD0-RD3, RDM, SBM, and ADM. The leading edge of this strobe will cause the user to provide valid data to be latched by Port Y by the trailing edge of IS.
Z2, Z3		2-bit address port used for memory or device selection. Both lines will be preset to 00 by selection of this mode. They will retain the value of the previous RDx or WRx instruction so that each selection can respond to RDM, SBM and ADM. If, for example an I/O sequence consists of an RD3 followed by an ADM, Z3 and Z2 will be at 11 state by the RD3 and remain in that state for the ADM command. If the third I/O command is a WR0, the Z3 and Z2 will be placed to the 00 state.

Effect of RDx and WRx Instructions:

Z3	Z2	
0	0	RD0, WR0
0	1	RD1, WR1
1	0	RD2, WR2
1	1	RD3, WR3
No Change		RDM, ADM, SBM

(Positive True)

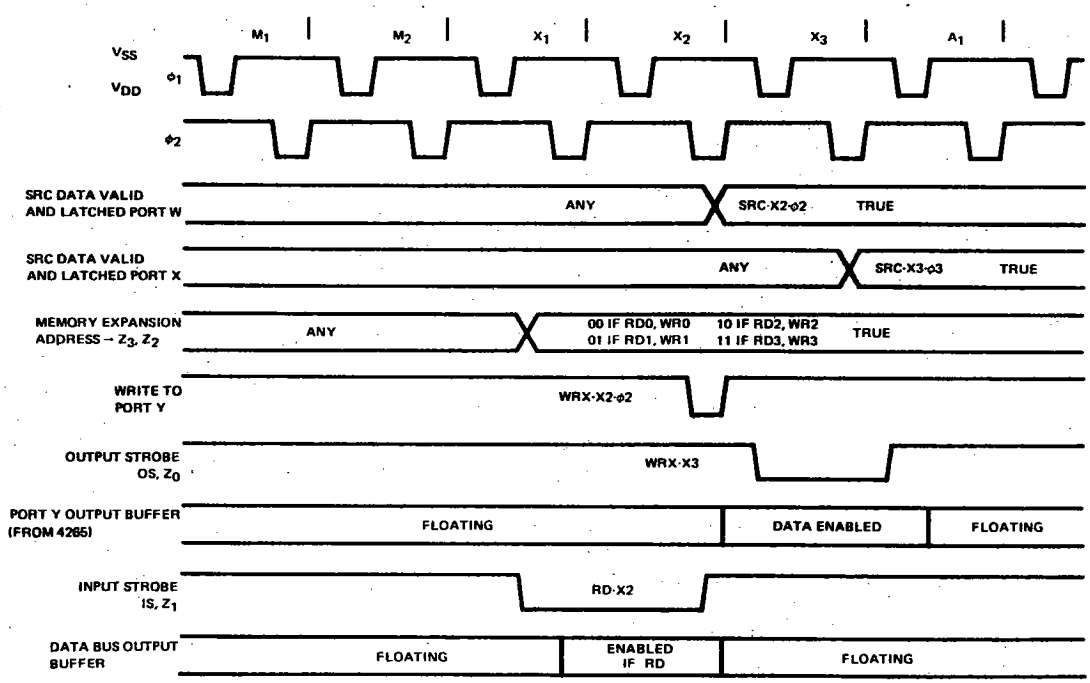


Figure 6. 4265 Mode 12 Timing.

h. 4-Bit I/O Mode with 8-Bit Address Port and 4-Bit Asynchronous Control Port – Mode 13

WMP Operand – 1101

Mode Description: This mode is functionally similar to Mode 12. Port W, X are loaded with the SRC value. Port Y is a bi-directional data port. Port Z is a 4-bit asynchronous control port similar to Mode 1 and 2.

Port Description

Port W, X		Same as Mode 12.
Port Y		Bi-directional port similar to Port W and Port X in mode 1.
Port Z		
Z0	OA*	Output acknowledge to 4265.
Z2	OI*	Output initiate from 4265, active during WRx.
Z1	II*	Input initiate to 4265.
Z3	IA*	Input acknowledge from 4265 active during RDx, RDM, ADM or SBM.

*Refer to Mode 1, Port Z. Note that in mode 13, Port Z controls data transmission in Port Y, not Ports W and X.

i. Disable/Enable

WMP Operands 1110 and 1111 do not cause mode change; they disable or enable the 4265 GP I/O.

WMP 1110 - chip disable:

a. All output buffers are disabled - I/O lines are in floating conditions.
b. The 4265's status (mode, chip select FF, data buffers) is not changed. Hence:
   1. Previous buffered inputs can be read by the CPU from designated ports (a disabled 4265 cannot have its input buffers loaded).
   2. Data on unbuffered inputs can be read directly from external lines.
   3. Previous buffered outputs can be changed on designated ports.
   4. Bit set/reset can be initiated.
   5. Any mode change can be initiated.
   6. The chip can be deselected by an SRC or by a RESET signal.

WMP 1111 - chip enable:
Restoration of normal operation, according to existing mode.

Note: When the 4265 is transferred from reset mode to any other mode, the chip is automatically enabled, so that no programmed enabling is required after reset.

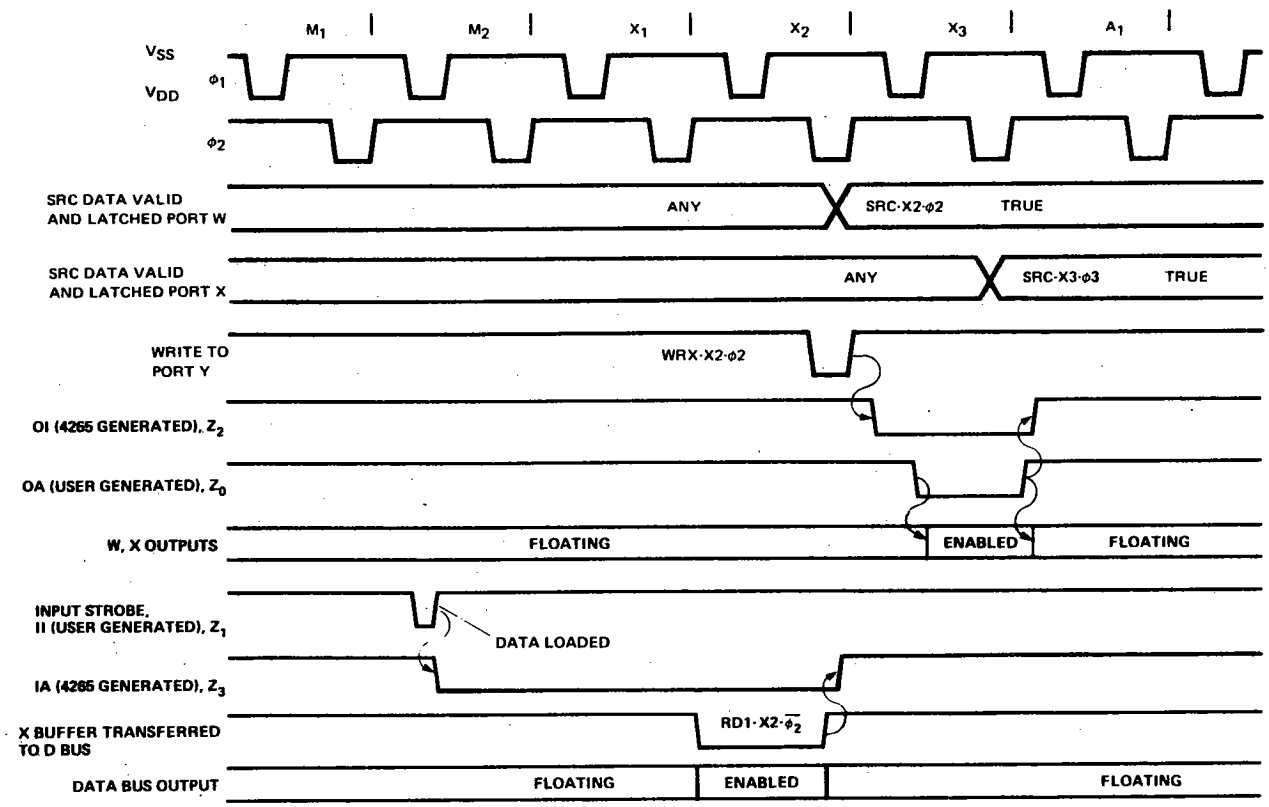


Figure 7. 4265 Mode 13 Timing.

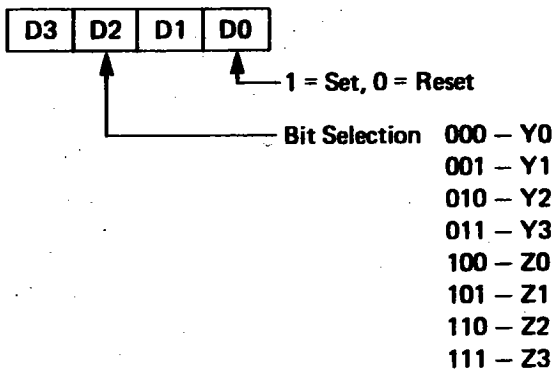
An unselected 4265 can have its input buffers loaded by a user generated strobe if it is in a buffered input mode. A disabled 4265 cannot have its input buffers loaded. Execution of a RDx instruction will result in transfer of the contents of the appropriate input or output buffer for a previously buffered port regardless of whether the 4265 is enabled. If the input was previously unbuffered and the 4265 is disabled, the contents of the port I/O lines will be transferred to the CPU with an RDx. DISABLE and ENABLE do not cause a change from a previously designated mode.

4265 States After Reset and Mode Change

A reset 4265 is automatically enabled and is in Mode 0. If reset occurs by means of external RESET signal, the 4265 will also be deselected. Any mode change which changes Port Z to a control port will reset the Port Z output buffers to their "off" state (V_{SS}). Z_2 and Z_3 in mode 12 are an exception in that these lines go to an inactive state of V_{DD1}. Note that Port Z is a control port in all modes except modes 4-7 and RESET mode. Any mode change which leaves Port Z in a non-control port will leave Port Z output buffers in their previous state.

Bit Set/Reset Operation

This function is performed by decoding the accumulator operand of the WRM instruction. This function can be used in any output port of the programmed configurations and allows individual bit control on Ports Y and Z. Decoding of the WRM operand is as follows:



Care should be taken when bit setting and resetting control bits of Port Z as these bits will also be changing as a function of their synchronous or asynchronous control functions.

4265 I/O Instructions

Table 2 provides a summary of MCS-40 I/O instructions used with the 4265.

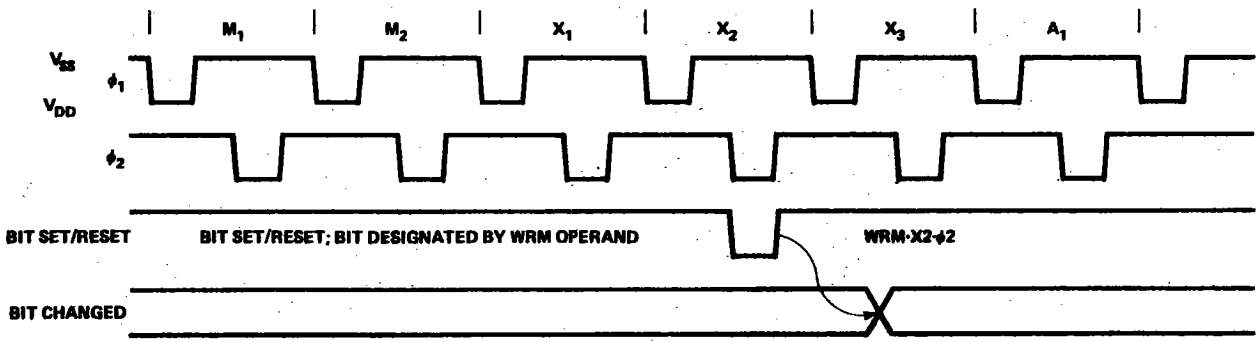


Figure 8. Bit Set/Reset Operation Timing.

Table 2. 4265 I/O Instruction.

Hex Code	MNEMONIC	OPR D_3 D_2 D_1 D_0	OPA D_3 D_2 D_1 D_0	DESCRIPTION OF OPERATION		
				Mode Independent Operations		
E0	WRM	1 1 1 0	0 0 0 0	The port Y or port Z bit designated by D_3 D_2 D_1 of the accumulator is set or reset according to D_0 (1=set, 0=reset).[1]		
E1	WMP	1 1 1 0	0 0 0 1	Sets the mode of the 4265 to the value contained in the accumulator.[2]		
				Mode Dependent Operations		
				Mode 1-3	**Mode 0, 4-11**	**Mode 12 and 13**
2-	SRC	0 0 1 0	R R R 1	For modes 0-11, the contents of register pair RRR are used to select the 4265 chip (first two bits of first register will contain 10 or 11, depending on chip address)		(RRR_{even})→ Port W (RRR_{odd})→ Port X
E4	WR0	1 1 1 0	0 1 0 0	(ACC)→ Port W	(ACC)→ Port W[1]	(ACC)→ Port Y
E5	WR1	1 1 1 0	0 1 0 1	(ACC)→ Port X	(ACC)→ Port X[1]	(ACC)→ Port Y
E6	WR2	1 1 1 0	0 1 1 0	(ACC)→ Port Y[1]	(ACC)→ Port Y[1]	(ACC)→ Port Y
E7	WR3	1 1 1 0	0 1 1 1	—	(ACC)→ Port Z[1,3]	(ACC)→ Port Y
EC	RD0	1 1 1 0	1 1 0 0	(Port W)→ ACC	(Port W)→ ACC	(Port Y)→ ACC
ED	RD1	1 1 1 0	1 1 0 1	(Port X)→ ACC	(Port X)→ ACC	(Port Y)→ ACC
EE	RD2	1 1 1 0	1 1 1 0	(Port Y)→ ACC	(Port Y)→ ACC	(Port Y)→ ACC
EF	RD3	1 1 1 0	1 1 1 1	(Port Z)→ ACC	(Port Z)→ ACC	(Port Y)→ ACC
E9	RDM	1 1 1 0	1 0 0 1	(Port Y)→ ACC	(Port Y)→ ACC	(Port Y)→ ACC
EB	ADM	1 1 1 0	1 0 1 1	(Port Y)+(ACC) +CY→ACC	(Port Y)+ACC +CY→ACC	(Port Y)+ACC +CY→ACC
E8	SBM	1 1 1 0	1 0 0 0	(ACC)−(Port Y) −CY→ACC	(ACC)−(Port Y) −CY→ACC	(ACC)−(Port Y) −CY→ACC

NOTES:
1. Action if Port is designated as Output Port; otherwise, no action.
2. WMP 1110 disables all I/O ports. WMP 1111 enables all I/O ports. In both cases, the mode is not changed.
3. No action in Modes 8-11.

Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -55°C to + 125°C
Input Voltages and Supply Voltage
with respect to Vss ..... +0.5V to -20V
Power Dissipation ..... 1.0 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400nsec; $t_{\phi D2}$ = 150nsec; V_{DD1} = V_{SS} -5V; Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless Otherwise Specified.

SUPPLY CURRENT

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_{DD}	Supply Current		35	50	mA	T_A = 25°C

INPUT CHARACTERISTICS

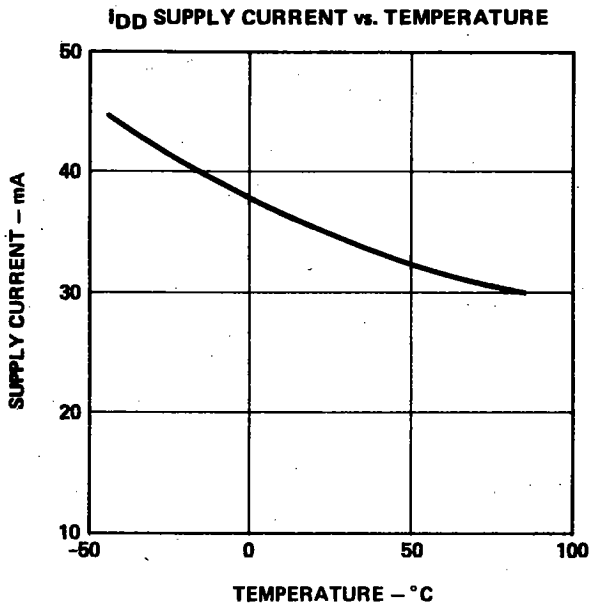
I_{LI}	Input Leakage Current			10	μA	
V_{IHD}	Data Bus Inputs	V_{SS}-1.5		V_{SS}+.3	V	
V_{IHIO}	I/O Port Inputs	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILD}	Data Bus Inputs	V_{DD}		V_{SS}-5.5	V	
V_{ILIO}	I/O Port Inputs	V_{DD}		V_{SS}-4.2	V	
$V_{IL/R,CM}$	Reset Input, CM-RAM Input	V_{DD}		V_{SS}-4.2	V	
$V_{IH/R,CM}$	Reset Input, CM-RAM Input	V_{SS}-1.5		V_{SS}+.3	V	
V_{IHC}	Input High Voltage Clock	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clock	V_{DD}		V_{DD}-13.4	V	

OUTPUT CHARACTERISTICS

V_{OHD}	Data Bus Outputs	V_{SS}-.5	V_{SS}		V	
V_{OHIO}	I/O Port Outputs	V_{SS}-.5			V	I_{OH} = -100μA
V_{OLD}	Data Bus Outputs	V_{SS}-12		V_{SS}-6.5		Capacitive Load
V_{OLIO}	I/O Port W,X,Y Outputs			V_{DD1}+.45		I_{OL} = 500μA
V_{OLZ}	I/O Port Z Outputs			V_{DD1}+.45		I_{OL} = 1.6mA
$R_{OH/D}$	Output Resistance, Data Bus High Level		150	250	Ω	V_{OUT}=V_{SS}-.5V
$R_{OH/IO}$	Output Resistance, I/O Port W,X,Y,Z High Level		1200	2000	Ω	V_{OUT}=V_{SS}-.5V
$I_{OL/WXY}$	I/O Port W,X,Y Sink Current	0.5			mA	V_{OUT}=V_{DD1}+0.45V
$I_{OL/Z}$	I/O Port Z Sink Current	1.6			mA	V_{OUT}=V_{DD1}+0.45V

CAPACITANCE

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_ϕ	Clocks ($\phi1, \phi2$)		10	15	pF	$V_{IN} = V_{SS}$. All other pins at V_{SS}.
$C_{D.B.}$	Data Bus		10	15	pF	
C_I	CM, RESET, SYNC		3	10	pF	
C_{WXY}	I/O Ports W,X,Y		5	10	pF	
C_Z	I/O Port Z		10	15	pF	



A.C. Characteristics

T_A = 0°C to 70°C, V_{SS} -V_{DD} = 15V ±5%.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t\phi_R$	Clock Rise Time			50	ns	
$t\phi_F$	Clock Fall Time			50	ns	
$t\phi_{PW}$	Clock Width	380		480	ns	
$t\phi_{D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
$t\phi_{D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500pF Data Lines
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT} = 20pF

I/O Ports ($C_{PORT\ W,X,Y}$ = 100 pF, $C_{PORT\ Z}$ = 50 pF)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{D0}	Output Settling Time		350	1200	nsec	Static Output Ports [1]
t_{D1}	Output Settling Time		400	1200	nsec	Ports W,X, Mode 1,2
t_{OH0}	Output Hold Time	80	400		nsec	Port Y, Mode 13
t_{D2}	Output Settling Time		400	1200	nsec	Ports W,X, Mode 3
t_{OH2}	Output Hold Time	550			nsec	Port Y, Mode 12
t_{D3}	O. S. Settling Time		300	650	nsec	Modes
t_{OH3}	O. S. Hold Time	550			nsec	3,8,9,10,12
t_{D4}	I. S. Delay		200	400	nsec	Z1, Modes 3,12
t_{DPS}	Page Select, Output Settling Time		250	550	nsec	Z2,Z3, Mode 12
t_{IS0}	Input Set Time	700	450		nsec	Unbuffered Input
t_{IH0}	Input Hold Time	100	-30		nsec	Ports W,X,Y
t_{IS1}	Input Write Time	900			nsec	Buffered Inputs (Ports
t_{IH1}	Input Hold Time	550			nsec	W,X Modes 1,2 Port Y Mode 13)
t_{DSR}	Bit Set/Reset Settling Time			900	nsec	
$t_{DOI/IA}$	OI,IA Delay Time			950	nsec	Z2,Z3, Modes 1,2,13 [2]
t_{PWII}	II Width			450	nsec	Modes 1,2,13
t_{PWIS}	IS Width	650			nsec	Modes 9,10,11 (4265 generated)

Notes: 1. t_{D0}: all output ports, modes 4-10; Y port, modes 2, 3.
2. $t_{DOI/IA}$: the maximum delay of any OI, IA edge with respect to its generating signal (strobe edge, clock edge, etc.). Refer to Figure 11 for generating signals and timing diagram.

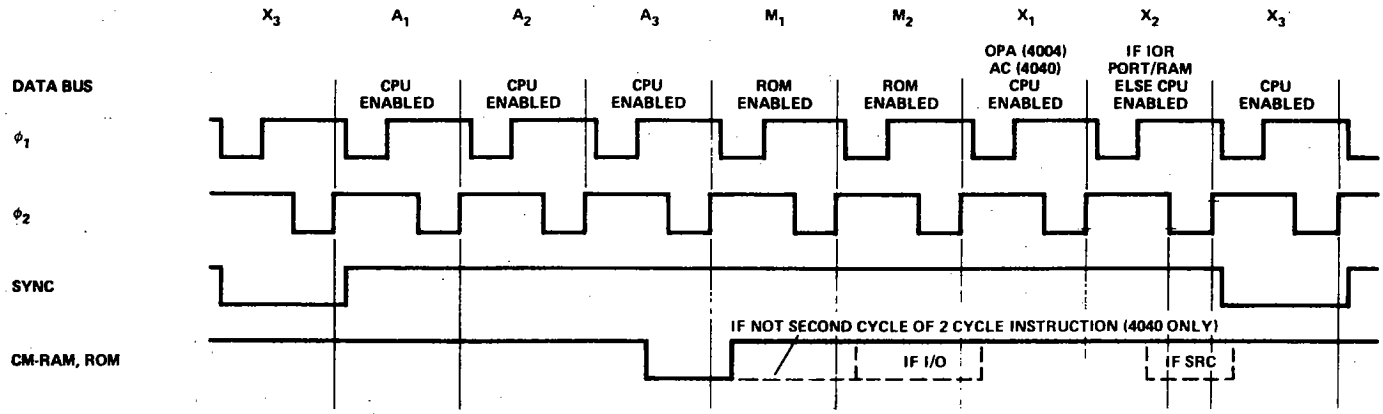


Figure 9. Timing Diagram.

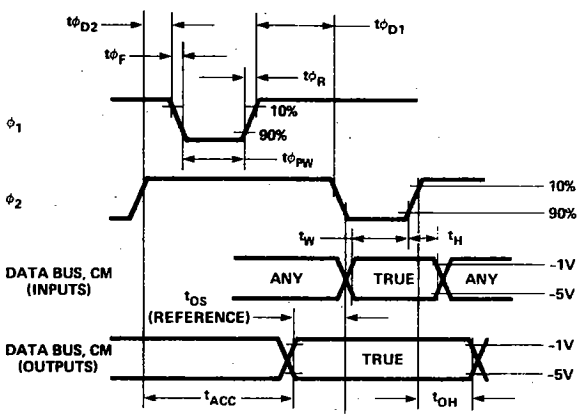


Figure 10. Timing Detail.

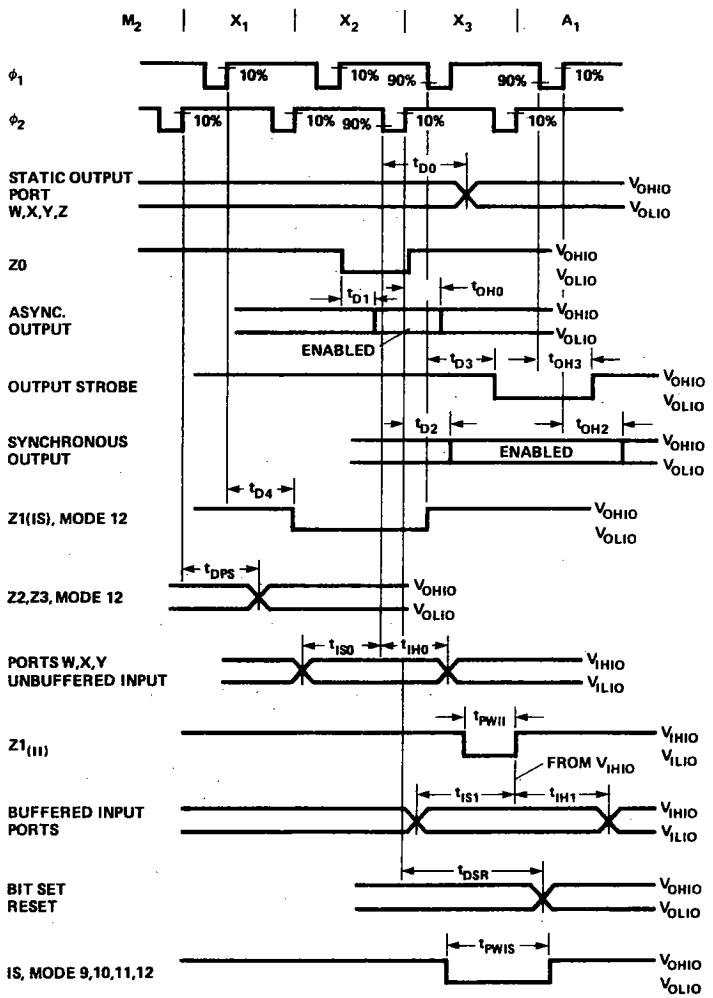


Figure 11. 4265 I/O Timing Diagram.

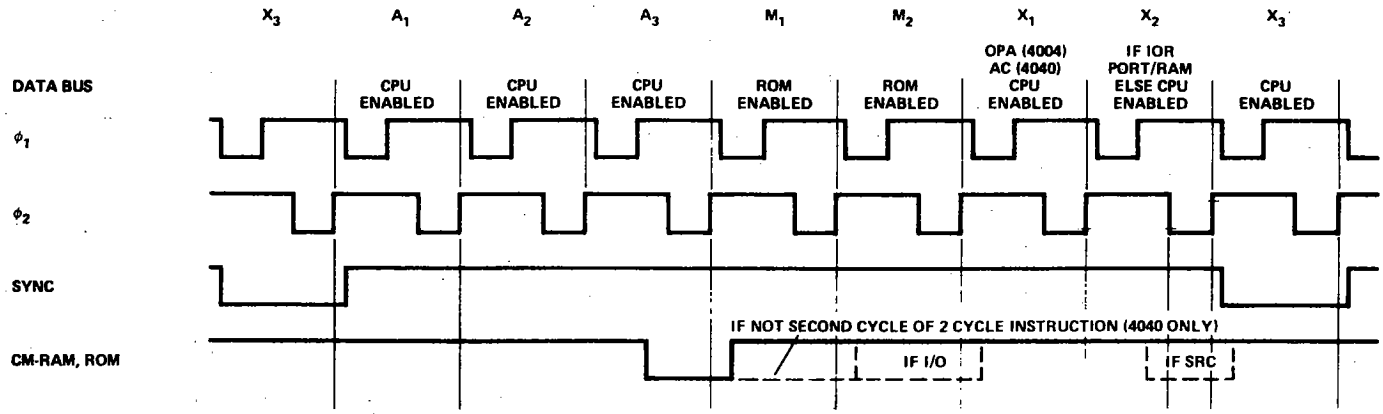


Figure 9. Timing Diagram.

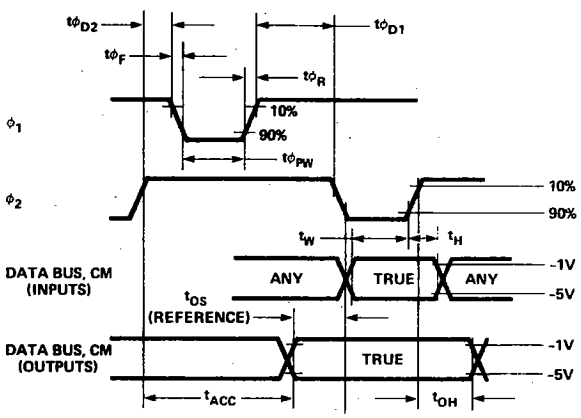


Figure 10. Timing Detail.

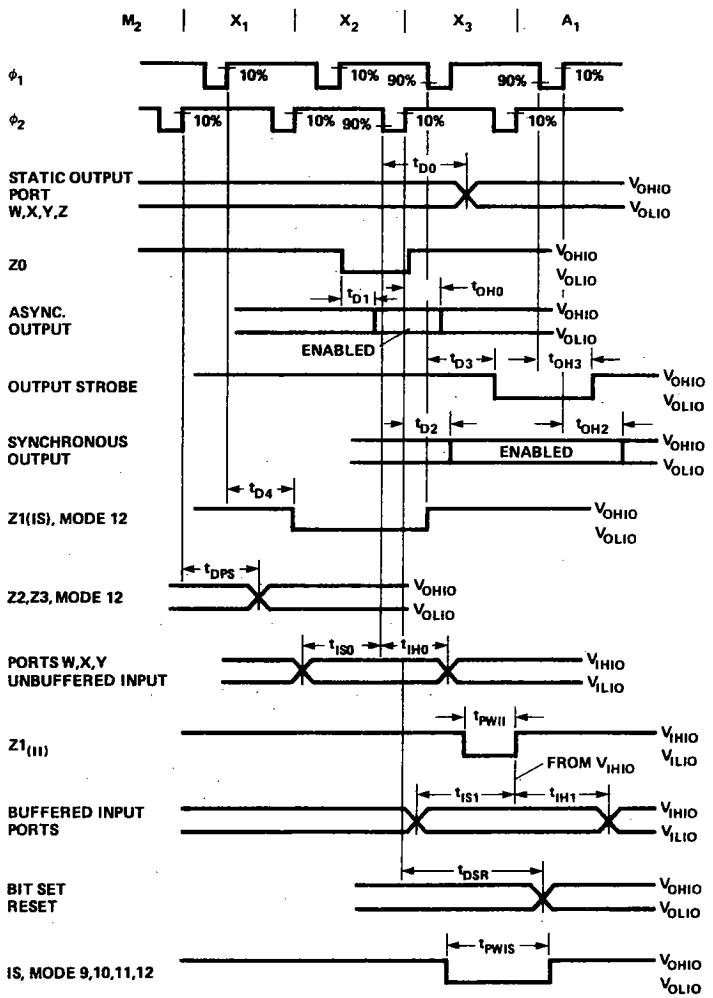


Figure 11. 4265 I/O Timing Diagram.