intel®

4269
PROGRAMMABLE KEYBOARD DISPLAY DEVICE

Keyboard Features:

- Programmable to Interface to Encoded Keyboard (8-bit code), 64-Key Scanned Keyboard (expandable to 128 keys) or Sensor Matrix (64 sensors)
- 8 Character FIFO Character Buffer (or RAM in Sensor Mode)
- 2 Key Rollover and Key Debounce
- External Interrupt Line to Indicate When a Character Has Been Entered in Character Buffer

Display Features:

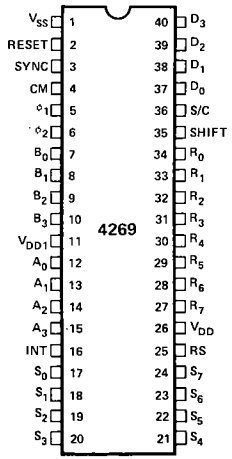
- Programmable to Interface to Individually Scanned Displays or Burrough's Self-Scan* Drive (16, 18, or 20 Characters)
- Two 16 x 4 Display Registers Recirculated Synchronously with Keyboard Scan Lines to Give Automatic Display Refresh
- Display Registers Loadable and Readable Selectively or Sequentially
- 40 Pin Dual In-Line Package
- Standard Operating Temperature Range of 0° to 70°C
- Also Available with -40°C to +85°C Operating Range

The 4269 has two separate and distinct sections: the keyboard section and the display section. The keyboard section can interface to a range of devices from a matrix of toggle or thumb switches such as found on an instrument panel up to a full typewriter style keyboard. The display section can interface to a range of devices from an array of individual LED indicators up to a gas discharge alphanumeric display.

The 4269 Programmable Keyboard Display (PKD) relieves the 4004 or 4040 CPU from continuously scanning a switch array or refreshing a display under software control. This greatly expands the CPU throughput. The 4269 can scan up to an 8 x 8 keyboard or sensor matrix (or a 2 x 8 x 8 keyboard with the use of the shift or control key input). The display portion can continuously refresh either a single 16 x 8 alphanumeric display; a single 8 x 8 alphanumeric display; a dual 16 x 4 digit display; a single 32 x 4 digit display; a 16 x 6, 18 x 6 or 20 x 6 alphanumeric gas discharge display such as the Burroughs Self-Scan*; or an array of 128 indicators.

*Self-Scan is a registered trademark of the Burroughs Corporation.

PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Designation	Function
37-40	D0-D3	Bi-directional data bus. All address, instruction and data communication between the CPU and the PKD are transmitted on these 4 pins.
5-6	ϕ_1-ϕ_2	Non-overlapping clock signals which are used to generate the basic chip timing.
2	RESET	RESET input. A low level (V_{DD}) applied to this input resets the PKD.
1	V_{SS}	Most positive supply voltage.
26	V_{DD}	Main power supply pin. Value must be V_{SS} - 15V ±5%.
3	SYNC	Synchronization input signal driven by SYNC output of the CPU.
4	CM	Command input driven by a CM-RAM output of processor.
17-24	S0-S7	These pins are scan outputs which are used for driving either the key switch or sensor matrix and/or for strobing the display digits. Each line is mutually exclusive, active high (V_{SS}), open drain.
25	RS	The RS pin is toggled for each complete scan of the S drive. This allows for the scan of 16 digits of display data. RS=V_{SS} for the last 8 digits. This line is open drain.
12-15 7-10	A0-A3 B0-B3	These two ports provide two 16 x 4 recirculating display register outputs which are synchronized to the S drive scan. In the gas discharge display mode, A3 is reset and A2 is the clock to the gas discharge display. The 16, 18, or 20 recirculating data characters (6 bits wide) are not synchronized with the S drive scan in the gas discharge mode. These lines are active high.
34-28	R0-R7	These pins are the return sense inputs which are connected to the 8 drive lines via the scanned key or sensor matrix. They are pulled to a low state (V_{DD}) in the sensor mode, pulsed low (V_{DD}) in the scanned keyboard mode, and pulled high upon switch closure. They are floating in the encoded keyboard mode.
35	SHIFT	This is the shift input. It is active high (V_{SS}). This pin is functional only in the scanned keyboard mode.
16	INT	This output is used to indicate when a keyboard or sensor character has been entered into the buffer. It is active low (V_{DD1}), open-sourced and may be "OR" -ed with other 4040 interrupt inputs.
11	V_{DD1}	Supply voltage for display register ports A and B and INT.
36	S/C	This pin is the control key input from the keyboard in the scanned mode. In encoded keyboard mode, this pin is used to input the strobe pulse from an external keyboard encoder. The strobe is an active high pulse.

FUNCTIONAL DESCRIPTION

General

The 4269 Programmable Keyboard/Display (PKD) device provides an intelligent interface between an MCS-40 CPU and the keyboard and display portions of an MCS-40 design. The 4269's functions thus allow the use of sophisticated keyboards and displays without placing a large load on the CPU.

The MCS-40 data bus will provide the path for information transfer between the PKD and the 4040 or 4004 CPU. The PKD can be programmed to operate in one of three input modes and one of four output modes as defined by an instruction from the CPU. The modes are:

Input	Sensor, Scanned Keyboard, Scanned Encoded Keyboard
Output	Individually Scanned Display Drive Self-Scan Drive: 16 Characters 18 Characters 20 Characters

The 4269 resides on a CM-RAM line of an MCS-40 system and has a fixed RAM address, #1. Hence, there can be up to four PKD per system without additional logic, one per CM-RAM. The PKD can be accessed with the MCS-40 I/O instruction set to interrogate the keyboard buffer FIFO/sensor RAM and load or read the display registers.

The following is a list of the major keyboard features of the 4269:

1. Switch matrix, organized as an 8 x 8 scanned matrix with shift or control inputs allowing for up to 128 key inputs.
2. Two key roll over; N-key roll over capability if provided by encoded keyboards.
3. Eight character first-in-first-out (FIFO) character buffer (or RAM in the Sensor Mode).
4. External interrupt line to indicate when a character has been entered in the buffer.
5. Fixed key bounce delay of approximately 11 msec in the scanned keyboard mode @ 740 kHz MCS-40 clocks.
6. Status buffer to indicate the number of characters in the keyboard FIFO and keyboard character over-entry.
7. Sensor matrix interface with up to 64 intersections.

The 4269's major display features are:

1. Two 16 x 4 display registers which are recirculated synchronously with keyboard scan lines (at a scan frequency of 180 Hz). This allows for a free standing, scanned readout composed of individual displays.

2. Capability to drive 16, 18, or 20 character gas discharge displays directly via a 20 x 6 display register.
3. Registers are loadable and readable selectively or sequentially.

Mode Selection

The CPU communicates with the 4269 PKD by first selecting it with an SRC (Send Register Control) instruction. The first two bits of the index register pair referenced by the SRC contain 01, the binary address of the 4269 on the CM-RAM line. The 4269 is disabled until it is addressed by a first SRC. After the first SRC, a WR0 instruction is used to set the keyboard and display modes of the 4269 PKD. The CPU's accumulator will contain the information used for setting the PKD modes. The definition of a WR0 as used for a 4269 is given below:

Mnemonic	Instruction Code
WR0	**1110 0100**

Set the input mode and output mode of the 4269 according to the value contained in the accumulator as follows:

D_3D_2

0 0 Individual, Scanned Displays
0 1 Gas Discharge, 20 Characters
1 0 Gas Discharge, 18 Characters
1 1 Gas Discharge, 16 Characters

D_1D_0

0 0 Sensor, Scanned
0 1 Scanned Keyboard
1 0 Encoded Keyboard, Not Scanned
1 1 Not Used

After the 4269 has been reset by the external RESET signal, the keyboard input mode is set to scanned keyboard mode and the display output mode is set to gas discharge, 16 character mode. Thus, if these modes are the desired input and output modes, it is not necessary to execute the WR0 mode setting instruction.

Internal Display Registers and Pointer

The 4269 has two 16x4 display registers referred to as Display Register A and Display Register B. These two registers can be operated in the individual, scanned display mode as:

1. Two 16 x 4 hexadecimal displays;
2. One 32 x 4 hexadecimal display;
3. One 8 x 8 alphanumeric display;
4. One 16 x 8 alphanumeric display; or
5. An array of 128 indicators.

In the gas discharge modes, the A and B registers are combined and operated as a 6 x 16, 6 x 18 or 6 x 20 register. For a given 6-bit character, the least significant 4-bits will be located in a 4-bit B register location and the two most significant bits in D_1 and D_0 of the corresponding A register location.

For operations on the display registers, the 4269 PKD maintains an internal display register pointer which points to a 4-bit character in the A or B display register.

For the individual, scanned display mode, CPU I/O instructions can be addressed to either Display Register A or Display Register B, according to the register selected by an SRC instruction preceding the I/O instruction. The internal display register pointer can then be set or incremented for addressing characters in either the A or B register.

For gas discharge modes, the internal pointer can be automatically incremented, in an alternating pattern between registers A and B. The alternation pattern is A_0, B_0, A_1, B_1, etc.

In the individual, scanned display mode, the 4-bit characters of Display Register A are outputted on the A_0-A_3 lines. The 4-bit characters of Display Register B are outputted on the B_0-B_3 lines. In the gas discharge modes, the A_0-A_1 and B_0-B_3 lines output the 6-bit character. The A_2 line serves as the clock to the gas discharge display and the A_3 line as the reset to the display.

Synchronization of Scan and Return Lines

In the scanned keyboard and scanned sensor modes a logical one is shifted through a field of zeros in eight Scan(S) lines. Each S Scan line can be used to source a row of eight keys or sensors. All rows of the contact keyboard or sensor matrix will be OR-tied to the eight Return (R) lines. Thus, since only one row will be enabled due to the synchronized ones in the Scan lines, each row of the keyboard or sensor matrix can be read into the Return lines and stored in the Keyboard FIFO/Sensor RAM at the proper RAM location. The 4269 will control all of these operations automatically once it is set to the appropriate keyboard mode.

The Scan Lines are also used in the individual, scanned display mode to select one of eight display characters. The display character itself will be outputted on the A_0-A_3 or B_0-B_3 output lines. The RS output line, which is toggled for each complete scan of the S lines, allows one of sixteen A or B register display characters to be addressed. Again, the 4269 will automatically control the operation of the S and RS lines to continuously read out the characters in the 4269's internal A and B Display Registers and thus continuously refresh the actual display devices.

Note that the Scan lines can be used with both the keyboard and display interfaces since both functions require the same function, i.e., a synchronized shifting of a logical one through a field of zeros.

Software Operation

The WR0 operates on the 4269 PKD completely independent of mode as it actually sets the mode as has already been described. The WR3 is mode independent except for a blanking code and operates as shown below:

WR3

Clears the keyboard/display logic and fills the display RAM with all blanks. The display outputs are also blanked. (Blank code is all logical "1"s for individual, scanned display mode and hex 20 for the gas discharge modes.)

MODE SPECIFIC OPERATIONS

Individual, Scanned Display Mode

The instructions which are used in the individual, scanned display mode are described below:

Mnemonic **Instruction Code**
SRC **0010** **RRR1**

The contents of the register pair RRR are used to select the 4269. An SRC is interpreted for individual, scanned display mode as follows:

RRR_{even}	RRR_{odd}	
$D_3D_2D_1D_0$	$D_3D_2D_1D_0$	
0 1 0 0	$n_3n_2n_1n_0$	Selects one of 16 display register characters of Display Register A with A outputs continuing to output the contents of Display Register A synchronized with the S Scan lines.
0 1 0 1	$n_3n_2n_1n_0$	Selects one of 16 display register characters of Display Register B with B outputs continuing to output the contents of Display Register B synchronized with the S Scan lines.
0 1 1 0	$n_3n_2n_1n_0$	Selects one of 16 display register characters of Register A and places the A output lines at V_{SS} level (blank). Display RAM contents are not modified.
0 1 1 1	$n_3n_2n_1n_0$	Selects one of 16 display register characters of Register B and places the B output lines at V_{SS} level (blank). Display RAM contents are not modified.

WR1 **1110** **0101**

Resets the internal display register pointer to 0 and forces display memory to blank state. Upper two bits of ACC select length of display as follows:

D_3

0 Display B is 16 nibbles deep.
1 Display B is 8 nibbles deep.

D_2

0 Display A is 16 nibbles deep.
1 Display A is 8 nibbles deep.

WRM **1110** **0000**

Loads the contents of the register addressed by the internal display register pointer with the contents of ACC; then advances the displayed data by one digit in relation to the scan line timing and increments the display register pointer.

RDM **1110** **1001**

Loads ACC with the contents of the register addressed by the display register pointer and then increments the display register pointer.

WMP **1110** **0001**

Loads the contents of the register addressed by the display register pointer with the contents of ACC.

RD3 **1110** **1111**

Loads ACC with the contents of the display register pointed to by the display register pointer.

ADM **1110** **1011**

Adds the contents of the display register pointed to by the display register pointer to the accumulator with carry.

SBM **1110** **1000**

Subtracts the contents of the display register pointed to by the display register pointer from the accumulator with borrow.

NOTES:

1. If Display A or B is set to 8 nibbles deep, each digit of the display will have double the ON duty-cycle that it would have in the 16 nibble deep setting (360 Hz scan cycle vs. 180 Hz for 16 nibble deep).
2. External resetting initializes the Display A and Display B configurations to 16 nibbles deep and blanks the display outputs.
3. The displayed nibbles in the 8 deep configuration will be from the least significant 8 characters of the display register. The remaining eight words remain available for random data storage by the CPU.
4. The internal display register pointer will increment through all 16 register words, regardless of the display length (8 or 16) for WRM/RDM instructions unless the pointer is reset by an appropriate SRC instruction. In the WRM case, the Display Register A or B's entire contents (used and unused portions) will be rotated.
5. An interface to a 32 x 4 hexadecimal display requires only that software recognize the A and B Display registers as the upper and lower halves of a single display.
6. An interface to a 16 x 8 alphanumeric display requires that software load the upper and lower 4-bits in the A and B registers in an appropriate alternating pattern. SRC instructions will have to proceed each load or read instruction to select the A or B half of the character.
7. If the LSD of a 16 character display is assigned to be the 15th character scanned ($S_7 = V_{SS}$ and RS = V_{SS}), and the MSD, the first character (#0) scanned ($S_0 = V_{SS}$ and RS = V_{DD}), and if loading is started at display register character 0, successive WRM instructions will shift the display data from the LSD to the MSD as in a calculator. Note that data will then be read back MSD to LSD with the RDM instruction, starting at register 0.

Gas Discharge Modes

The instructions which are used in the gas discharge display modes are described below.

Mnemonic **Instruction Code**
SRC **0010** **RRR1**

The contents of the register pair RRR are used to select the 4269. An SRC is interpreted for gas discharge modes as follows:

RRR_{even}	RRR_{odd}	
$D_3D_2D_1D_0$	$D_3D_2D_1D_0$	
0 1 0 0	$n_3n_2n_1n_0$	Selects the nth display register character of Display Register A with display outputs continuing to output the contents of Display Registers A and B.
0 1 0 1	$n_3n_2n_3n_0$	Selects the nth display register character of Display Register B with the display outputs continuing to output the contents of Display Registers A and B.
0 1 1 0	$n_3n_2n_1n_0$	Selects the nth display register character of Display Register A and blanks the A and B display output (with hex 20) with no modification of display RAM contents.
0 1 1 1	$n_3n_2n_1n_0$	Selects the nth display register character of Display Register B and blanks the A and B display output (with hex 20) with no modification of display RAM contents.

WR1

Resets the internal display register pointer to Display Register A position 0 and forces the Display Registers to the blank code.

Note: A WR1 should follow a WR0 which changes the display mode.

WRM 1110 0000

Loads the contents of the display register location addressed by the internal display register pointer with the contents of ACC; then advances the displayed data by one digit in relation to the scan line timing, and increments the display register pointer. The display register pointer alternates between the A and B registers.

RDM 1110 1001

Loads ACC with the contents of the display register location addressed by the display register pointer and then increments the display register pointer. The display register pointer alternates between the A and B registers.

WMP 1110 0001

Loads the contents of the display register location addressed by the display register pointer with the contents of ACC.

RD3 1110 1111

Loads ACC with the contents of the display register location pointed to by the display register pointer.

ADM 1110 1011

Adds the contents of the display register pointed to by the display register pointer to the accumulator with carry.

SBM 1110 1000

Subtracts the contents of the display register pointed to by the display register pointer from the accumulator with borrow.

NOTES:

1. The alternation pattern of the display register pointer is Display Register A position 0, Display Register B position 0, Display Register A position 1, etc.
2. The upper two (four) gas discharge characters, 16-17 (16-19), can be addressed only by incrementing the internal display register pointer above 15 by a WRM or RDM instruction in 18 (20) character gas discharge mode. If the internal display register pointer has been incremented above 15, then these characters can be read or written by a RD3 or WMP instruction.
3. Successive WRM commands will shift the output data (see gas discharge display output format below) one character forward in relation to the reset pulse. This will cause a wraparound shift left on the self-scan display. Hence, starting at register 0 and loading the display RAM will give a right-justified display — MSD first.

	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0
	RST	CLK	D_5	D_4	D_3	D_2	D_1	D_0
BLANK CODE:	X	X	1	0	0	0	0	0

Figure 1. Gas Discharge Display Output Format.

4. RDM will not cause any display shifting. The read order is MSD to LSD with the MSD stored in display register 0.
5. If the display RAM is used as data RAM by the CPU, all 4 bits of Register A can be read and written, i.e., the A_3 and A_2 RAM positions are not actually modified in the RAM.

Scanned Sensor Mode

The instructions which are used in the scanned sensor mode are described below:

Mnemonic	Instruction Code	
SRC	0010	RRR1

The contents of the register pair RRR are used to select the 4269. An SRC is interpreted for scanned sensor mode as follows:

RRR_{even}	RRR_{odd}	
$D_3D_2D_1D_0$	$D_3D_2D_1D_0$	
0 1 X X	$n_3n_2n_1$ X	n_3-n_1 indicates an 8-bit sensor group to be read.

WR2 1110 0110

Clears the FIFO/RAM logic and the INT line.

RD1 1110 1110

Loads into ACC the upper 4 bits of the 8-bit sensor RAM group previously addressed by an SRC instruction.

RD2 1110 1110

Loads into ACC the lower 4 bits of the 8-bit sensor RAM group previously addressed by an SRC instruction.

NOTES:

1. In this mode, the 4269 PKD will continuously input the 64 matrix intersections of the sensor into the FIFO/Sensor RAM, which is organized as a 64-bit RAM.
2. The INT line will become active (V_{DD1}) and remain active whenever at least one intersection remains a logical one in the Sensor RAM.
3. The sensor group number set by the SRC is loaded into the internal display register pointer. Display mode instructions which change the internal display register pointer thus change the sensor group address.

Scanned Keyboard and Encoded Keyboard Modes

The instructions which are used in the scanned keyboard and encoded keyboard modes are described below:

Mnemonic	Instruction Code	
SRC	0010	RRR1

The contents of the register pair RRR are used to select the 4269. An SRC is interpreted as follows for scanned and encoded keyboard modes:

RRR_{even}	RRR_{odd}	
$D_3D_2D_1D_0$	$D_3D_2D_1D_0$	
0 1 X X	X X X X	SRC used only to select 4269.

WR2 1110 0110

Clears FIFO/RAM logic, the status buffer, and the INT line.

RD1 1110 1101

Reads the first nibble of the current FIFO register position.

RD2 1110 1110

Reads the second nibble of the current FIFO register position. FIFO register position is incremented to the next position.

RD0 1110 1100

Loads ACC with the FIFO status.

Notes:

1. The 4-bit FIFO status contains the number of valid characters (0-8) in the keyboard FIFO. However, in the event of an overrun, i.e., more than 8 characters entered, the 4-bit status will be set to a value of 15. The first eight characters entered prior to the overrun character will remain in the FIFO until cleared.
2. When a character is entered in the FIFO, the INT output pin wil go to V_{DD1}. When a character is read, the INT will change from V_{DD1} to V_{SS} (open) and back to V_{DD1} until the FIFO has been emptied. If a ninth character is inputted to the PKD before one complete character has been removed, the overrun status will be set. This will cause the INT line to remain active (V_{DD1}) even after all characters have been accessed. Overrun status can only be cleared by a WR2 or WR3 command (although the first eight FIFO characters can be read). This condition allows the user to detect an overrun condition if it occurs between the time the status buffer is checked and the time all characters have been read. It should be noted that an RD2 must be initiated after an RD1 to advance to the next FIFO word even if the second nibble is not desired.
3. For a 16-key Keyboard, successive RD2 instructions will be adequate for inputting the key code.

DESIGN CONSIDERATIONS

Display Modes

General Remarks

Each Display A and Display B output is capable of driving one standard TTL load. This is done by using a V_{SS} = +5, V_{DD} = -10V and V_{DD1} = GND. The V_{DD1} pin allows the PKD to interface to a variety of commercially available display arrays via a specified circuit. Gas discharge, phosphorescent, LED, and incandescent displays can all be used with a 4269. The interface requirements are determined by the selected display device. Current into each of the Display A and Display B output lines should not exceed 1.6mA.

The two 16 x 4 Display Registers A and B provide information in hexadecimal positive logic conventions. Hence, a 0000, negative logic V_{SS} on the data bus, will be 0000 (positive logic V_{DD1}) at the A and B display output. (The above is equivalent to one level inversion between the data outputs of the PKD and the CPU accumulator.)

Note that since the PKD is at address No. 1 on the CM-RAM line and that since the last 2 bits of the even register pair of an SRC instruction cause blanking or unblanking of the display and modification of the internal display register pointer, that addresses 01XX are not available for addressing other I/O ports on the same CM-RAM line as the one containing the PKD.

Individual, Scanned Display Mode

The digit selection is achieved by using the eight scan lines, S_0-S_7, and the display select line RS. The RS output is used to multiplex the eight scan strobes to give sixteen separate strobes for up to 16 digits of display.

It should be noted that the LSD output position of both Display Registers A and B is gated out coincidently with S_0 time of the scan register. Following digit positions are also coincident. This feature allows an interface to 8 x 8 or 16 x 8 displays. For the first eight display digit positions, the RS output is at open drain. The remaining eight of the 16 digit positions are output sequentially with RS at V_{SS}. Sufficient active on-time (V_{SS}) is allowed at the scan strobe line (S_0-S_7) to illuminate the displayed digit. Sufficient time is also allowed between segments to extinguish segment and prevent overlapped illumination. If the 8 digit mode is selected with the WR1 instruction, the LSD will be gated out every S_0 time – not every other time.

For an aesthetic display transition, the display register outputs can be placed into the blank mode (all outputs to V_{SS}) via an SRC during the loading of the display register. The outputs can then be unblanked via another SRC when the display register has been completely loaded.

Gas Discharge Modes (Self-Scan)

An approximate 100 μsec period, 50% duty cycle clock will be provided to the gas discharge display. A reset pulse – one clock period long – will be generated every 112th clock period for the 16/18 digit displays or every 140th clock period for 20 digit displays. Character periods are either seven clock periods long (for 16 or 20 character displays) or six clock periods long (for 18 character displays). For either case, character data is valid for the first five clock periods of the character period. Character 0 (left-most digit) starts upon the rising edge of the reset signal. The blank code is $A_1 = V_{SS}$ and A_0, B_3 - $B_0 = V_{DD1}$, with A_3 and A_2 providing reset and clock functions respectively. For the 18 character gas discharge display mode, the data outputs are blank for the 108th, 109th, and 110th clock periods.

Keyboard Modes

Scanned Sensor Mode

The sensor interface consists of two groups of eight lines, the scan strobe lines (S_0-S_7) and the return sense lines (R_0-R_7). Each scan strobe is used to enable eight return lines, giving 64 total sense strobes for each complete scan. When in the sensor mode, the two key rollover and debounce logic is inhibited. This allows multiple valid intersection connections to be inputted. The SHIFT and S/C (CONTROL) inputs are ignored in this mode.

Each sensor intersection will have a RAM location reserved. The designer should group the sensors in common groups of 4. This mode is intended to be used to scan a matrix of electronic intersections or mechanical contacts. Debouncing is to be performed under software control. The INT line will remain active (V_{DD1}) whenever a valid intersection has been detected. The scan strobe cycle is the same pattern of a logical 1 (V_{SS}) shifted in a field of zeros.

The sense return lines are read out by RD1/RD2 instructions as shown in Figure 2.

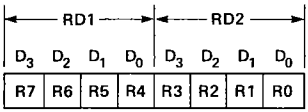


Figure 2. Sense Return.

If scanned sensor mode and individual, scanned display mode are used together, the Scan (S) lines should be electrically isolated by diodes (see Figure 4).

Scanned Keyboard Mode

a. Key Depression Detection

These conditions can occur during the keyboard interrogation by the PKD (see timing diagram below).

1. Simultaneous Key Depression

   Two or more keys depressed within one complete single depression scan (approximately 11ms) is defined as a simultaneous key depression. If this condition occurs, the PKD continues to scan the keyboard and waits until one key remains depressed. It then treats the remaining key as a single key depression, as described below.

2. Single Key Depression

   When any single key (non-simultaneous) is depressed, an internal counter is started. The key code is also stored internally in a PKD temporary register with a code given by the values of the Scan and Return Lines. The PKD will then make four more complete scans of all keys. If no other keys are depressed during the fourth complete scan and the original key detected is still depressed at the end of the fourth scan, the key code is defined as a single key depression. The key code is then entered into the FIFO along with the value of the SHIFT and Control (S/C) input signals. If eight characters are already in the FIFO, the character will not be entered and the overrun will be set. When a character is entered in the FIFO, the INT line is activated to a logical "1" (V_{DD1}). If on the fourth complete scan the original key depressed is no longer depressed, the key is ignored as if it had never been depressed. This delay of four scan times, or approximately 11ms, thus provides the debounce function for the keyboard.

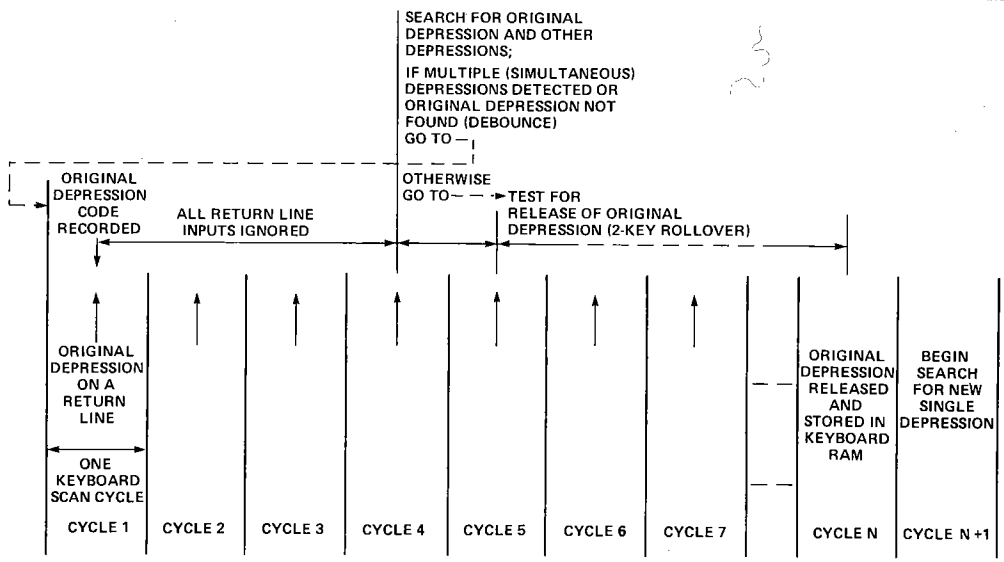


Figure 3. Keyboard Debounce and 2-Key Rollover Timing.

3. Two Key Rollover

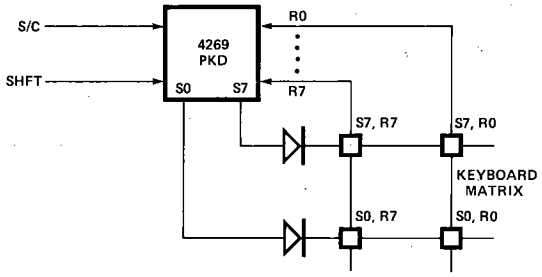
The two key rollover operates as follows:

If a second key is depressed after a first key has been accepted by the PKD as a single key depression but the first key has not been released, then the second key will be treated as a new original depression after the first key has been released.

If a second key is depressed after a first key has been accepted by the PKD as a single key depression and the second key is released before the first key is released, the second key will be ignored.

b. Key Matrix Encoding

The keyboard matrix hardware configuration and associated matrix encoding is shown in Figures 4, 5, and 6.



NOTE THAT ISOLATION DIODES MUST BE PLACED IN THE SCAN LINES AS SHOWN IF THE SCAN LINES ARE ALSO USED TO STROBE A DISPLAY. IF THE KEYBOARD USED HAS A DIODE AT EACH KEY, THEN THE SCAN LINE ISOLATION DIODES ARE NOT REQUIRED.

Figure 4. Hardware Configuration.

	R_0 000	R_1 001	R_2 010	R_3 011	R_4 100	R_5 101	R_6 110	R_7 111	SHIFT	S/C
S_0 000	0	1	2	3	4	5	6	7	X	X
S_1 001	8	9	10	11	12	13	14	15	X	X
S_2 010	16	17	18	19	20	21	22	23	X	X
S_3 011	24	25	26	27	28	29	30	31	X	X
S_4 100	32	33	34	35	36	37	38	39	X	X
S_5 101	40	41	42	43	44	45	46	47	X	X
S_6 110	48	49	50	51	52	53	54	55	X	X
S_7 111	56	57	58	59	60	61	62	63	X	X

Figure 5. Matrix Configuration.

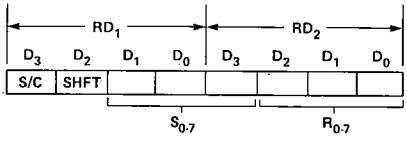


Figure 6. Key Encoding.

c. Expansion to 128 Key Scan

The basic mechanism of the PKD for scanning a 64 key matrix can be expanded to interface to a 128 key matrix. Note that the CONTROL (S/C) and SHIFT inputs cannot be used to directly encode 256 keys since the single key depression logic operates with the 6-bit matrix position code only. However, if full debounce and 2 key roll over control between two 64 key matrices is not necessary, then a configuration such as shown in Figure 7 may be used to add a seventh bit to the 6-bit matrix via the SHIFT or S/C input of the PKD. Alternately, two 4269 PKDs can be used for interfacing to the 128 keys.

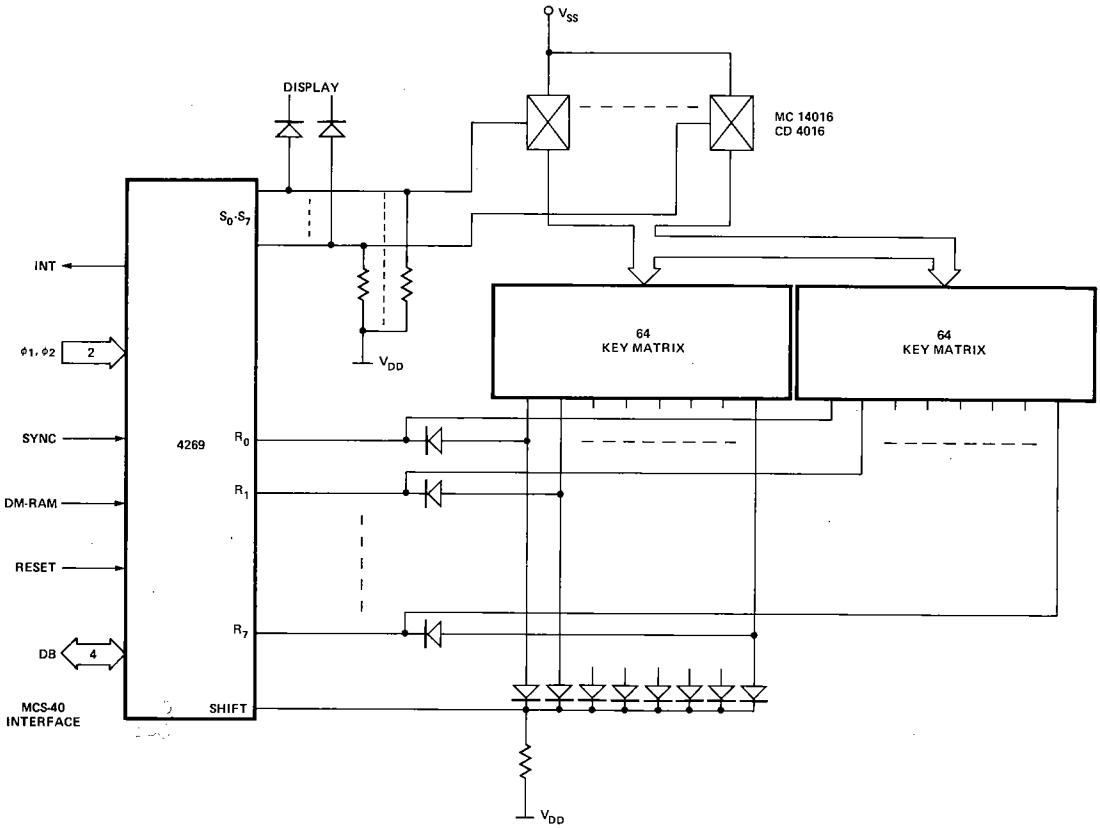


Figure 7. 128 Scanned Input Keys.

Encoded Keyboard Mode

Data Format

In the encoded keyboard mode, the eight return lines are directly loaded into the PKD's keyboard FIFO. For encoded keyboards using less than eight encoded bits, the remaining bits can be any desired signal, such as a multiplex signal between two keyboards or a special key flag.

HARDWARE DESCRIPTION

The following is a description of the major hardware elements of the 4269. Refer to the hardware block diagram shown in Figure 8.

MCS-40 Data Bus/Control Line Interface

The 4269 PKD resides on the MCS-40 data and timing bus. As such it derives its basic timing from the ϕ_1 and ϕ_2 clock signals. Synchronization and chip select information are provided by the SYNC and CM-RAM lines respectively. The Data Bus provides the 4269 with control commands and routes Keyboard/Display data between the 4269 and CPU Accumulator.

Display Registers

The 4269 is provided with RAM storage which is utilized to implement an automatically refreshed display. The display RAM (Display Registers A and B) can be configured in several different organizations under program control, including two 16 x 4 hexadecimal displays, one 32 x 4 hexadecimal display, a single 8 or 16 alphanumeric display, a single 16, 18, or 20 character gas discharge alphanumeric display, or a 128 matrix array of indicators. The display RAM output is available on A_0-A_3 for Display Register A outputs and B_0-B_3 lines for Display Register B outputs. The V_{DD1} line provides a separate negative supply reference for the A and B outputs (and INT).

S/R Counters and Debounce Logic

The S/R counters are two modulo 8 counters used to provide a unique 6-bit code for each of the 64 intersections provided by a matrix of eight Scan (S) Driver and eight Return (R) sense lines. The R counter is counted eight times for each S count. When keys, contacts, or controls are arranged in the matrix, each matrix intersection is examined for closure between the corresponding S and R line. If the 4269 is in the Scanned Keyboard Mode, an approximate 11 msec debounce time will be used to ascertain the validity of the connection. The valid 6-bit code, along with the SHIFT and S/C (control) line, is placed in the FIFO for retrieval by the CPU.

Scan Counter and Scan F/F

For each increment of the modulo 8 S counter, the Scan Counter is advanced. The register shifts a logical 1 (V_{SS}) in a field of logical zeros (open drain). The non-overlapping one is successively moved from S_0 through S_7 and around again. For each complete sequence of shifts, the scan flip-flop is toggled. This flip-flop's initial value, after RESET, is open drain.

Key Return Multiplexer

The return multiplexer selects one of the 8 return lines coming from the key array. The selection code is provided by the modulo 8 R counter. When in the Scanned Sensor Mode, all 8 R lines are entered for each scan line, and pass directly to the Sensor RAM (FIFO).

FIFO and Sensor RAM

This block is a dual function RAM of 64 bits. The RAM can serve as a keyboard character FIFO for eight 8-bit characters or as a sensor RAM to store the status of 64 intersections.

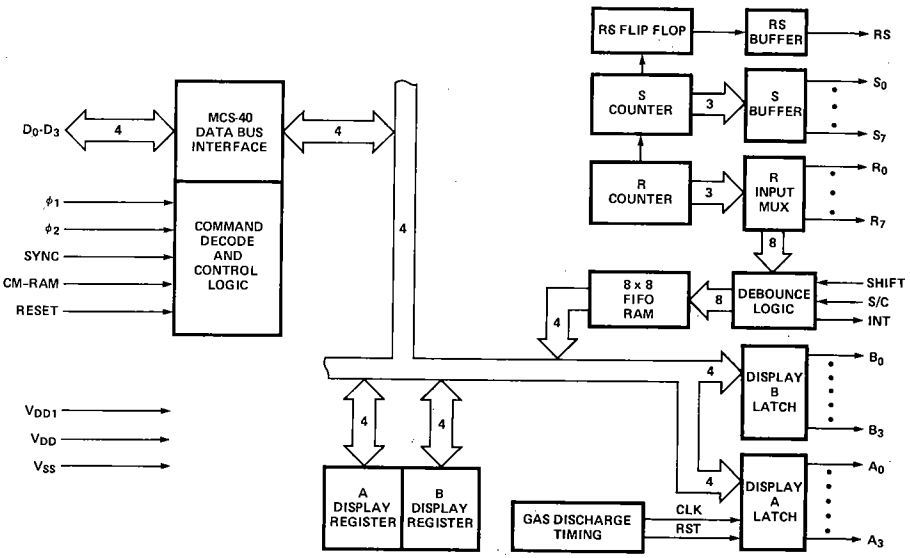


Figure 8. 4269 Hardware Block Diagram.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -55°C to + 125°C
Input Voltages and Supply Voltage
with respect to Vss ..... +0.5V to -20V
Power Dissipation ..... 1.0 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0° to 70°C; V_{SS} -V_{DD} = 15V ±5%; V_{DD1} = V_{SS} -5V; $t_{\phi PW}$ = $t_{\phi D1}$ = 400nsec; $t_{\phi D2}$ = 150nsec; Logic "0" is defined as the more positive voltage (V_{IH},V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL},V_{OL}); Unless Otherwise Specified.

SUPPLY CURRENT

Symbol	Parameter	Limits Min.	Typ.	Max.	Unit	Test Conditions
I_{DD}	Supply Current		40	65	mA	T_A = 25°C
I_{DD1}	V_{DD1} Current			15	mA	T_A = 25°C
INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	µA	V_{IL} = V_{DD}
V_{IL}	Input Low Voltage (Except Clocks, Return Lines, Shift, S/C)			V_{SS}-5.5	V	
V_{IL}	Input Low Voltage (Return Lines, Shift, S/C)	V_{DD}		V_{SS}-4.2	V	
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
OUTPUT CHARACTERISTICS						
I_{LO}	Data Bus Output Leakage Current			10	µA	V_{OUT} = -12V
I_{OL}	Data Bus Sinking Current	8	15		mA	V_{OUT} = V_{SS}
I_{OLAB}	A_{0-3}/B_{0-3} Sinking Current	1.6			mA	V_{OUT} = V_{DD1} +.4V
I_{OHAB}	A_{0-3}/B_{0-3} Drive Current	50			µA	V_{OUT} = V_{SS} -2.6V
I_{OLI}	Interrupt Sinking Current	200			µA	V_{OUT} = V_{DD1} +.4V
I_{OHS}	S Lines Driving Current	3.2			mA	V_{OUT} = V_{SS} -1.0V
I_{OHRS}	RS Line Driving Current	2.5			mA	V_{OUT} = V_{SS} -2.6V
R_{OH}	Data Bus Output Resistance		150	250	Ω	V_{OUT} = V_{SS} -.5V

MCS 4/40

A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$; $V_{SS} - V_{DD} = 15V \pm 5\%$.

Symbol	Parameter	Limits			Unit	Test Condition
		Min.	Typ.	Max.		
t_{CY}	Clock Period	1.35		2	μsec	
$t_{\phi R}$	Clock Rise Time			50	nsec	
$t_{\phi F}$	Clock Fall Time			50	nsec	
$t_{\phi PW}$	Clock Width	380		480	nsec	
$t_{\phi D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	nsec	
$t_{\phi D2}$	Clock Delay ϕ_2 to ϕ_1	150			nsec	
t_W	Data-In, CM, SYNC Write Time	350	100		nsec	
t_H[1,2]	Data-In, CM, SYNC Hold Time	40	20		nsec	
t_{OS}[3]	Set Time (Reference)	0			nsec	C_L = 500 pF
t_{ACC}	Data Bus Access Time			930	nsec	C_L = 500 pF
t_{OH}	Data Bus Hold Time	50			nsec	C_L = 20 pF
t_{RTSK}	Return Line Pull-Down Time		5	16	μs	C = 120pF; Scanned Keyboard Mode
t_{RTSN}	Return Line Pull-Down Time		30	200	μs	C = 120 pF; Sensor Mode

CAPACITANCE

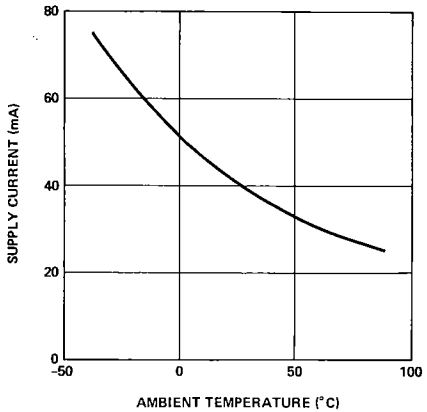
Symbol	Parameter	Limits			Unit	Test Condition
		Min.	Typ.	Max.		
C_ϕ	Clock Capacitance		8	25	pF	$V_{IN} = V_{SS}$
C_{DB}	Data Bus Capacitance		14	25	pF	$V_{IN} = V_{SS}$
C_{IN}	Input Capacitance			10	pF	$V_{IN} = V_{SS}$
C_{OUT}	Output Capacitance			15	pF	$V_{IN} = V_{SS}$

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.

2. All MCS-40 components which may transmit instruction on data to a 4004 or 4040 at M_2 and X_2 always enter a float state until the 4004/4040 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.

3. t_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} in the same output access time referred to the leading edge of the next ϕ_2 clock pulse.

TYPICAL I_{DD} SUPPLY CURRENT VS. TEMPERATURE



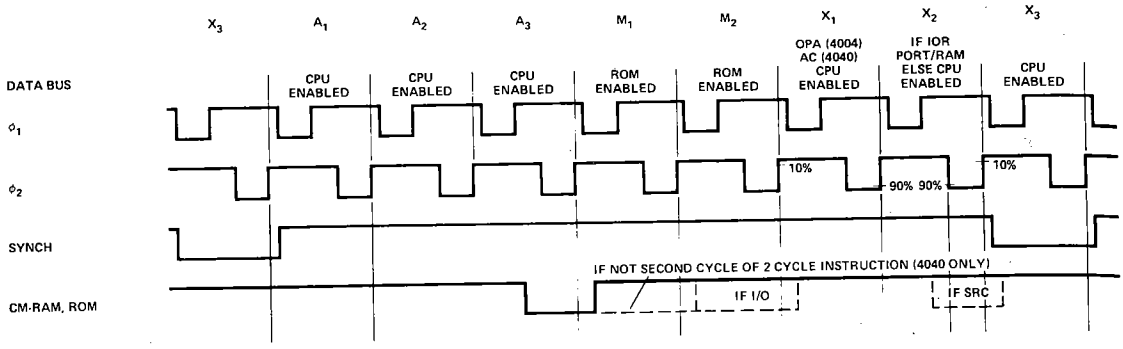


Figure 9. Timing Diagram.

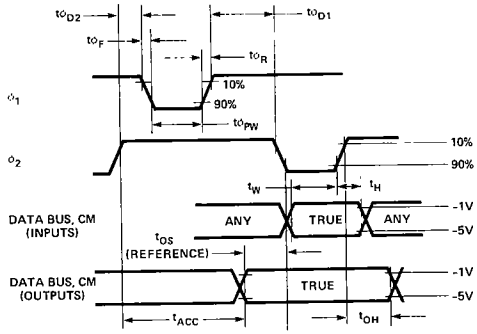


Figure 10. Timing Detail.

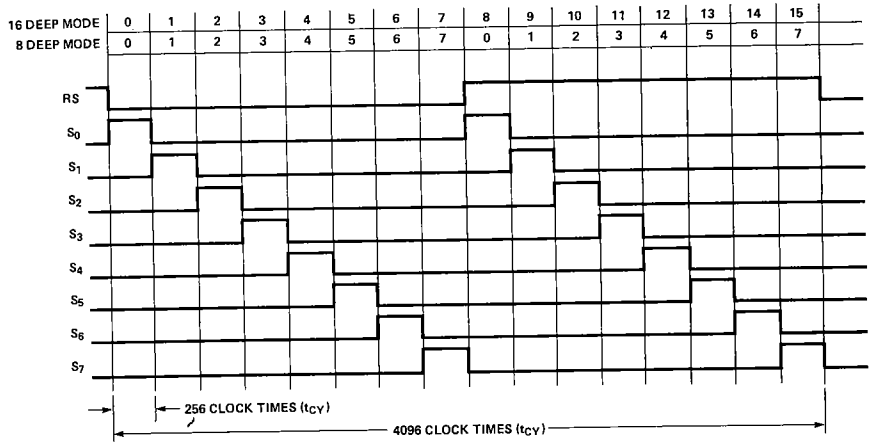


Figure 11. Individually Scanned Display Mode Timing After Execution of 0 or 16 WRM Instruction (or 8 WRMs for 8 Nibbles Deep Mode).

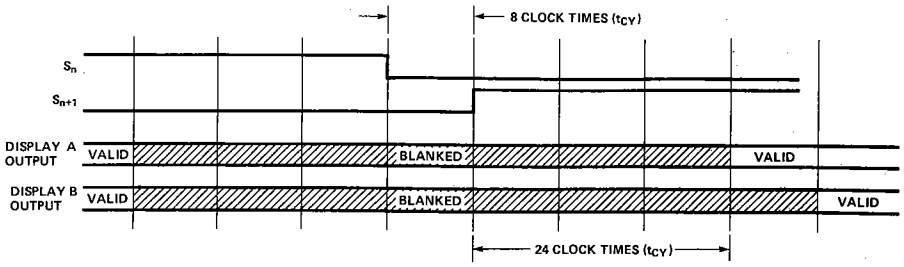


Figure 12. Individually Scanned Display Mode.

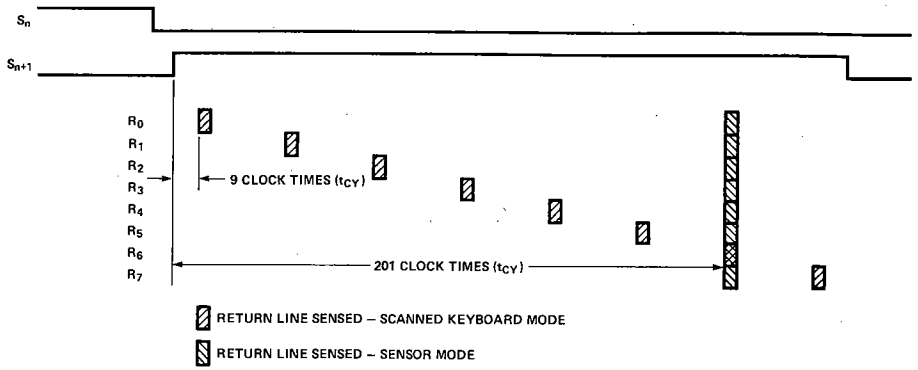


Figure 13. Return Line Timing for Scanned Keyboard and Sensor Mode.

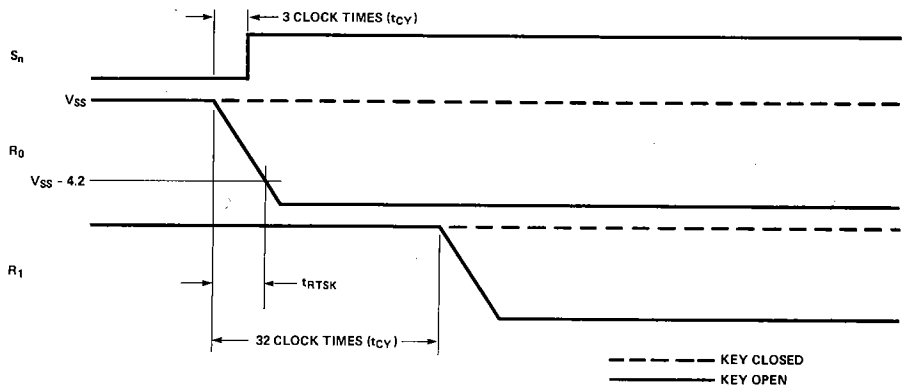


Figure 14. Detailed Timing – Scanned Keyboard Mode.

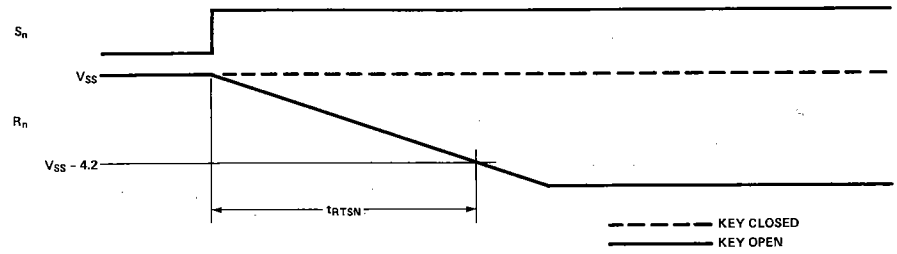


Figure 15. Detailed Timing – Sensor Mode.

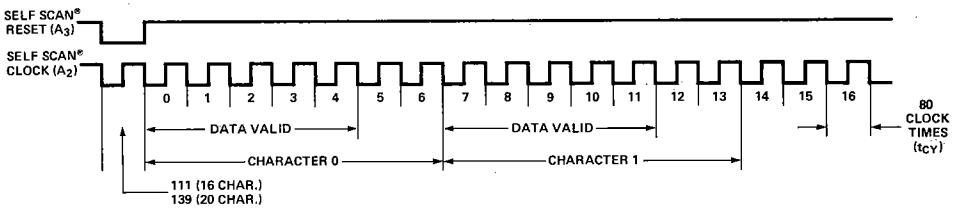


Figure 16. Gas Discharge (Self-Scan®) Mode Timing – 16 or 20 Character Mode.

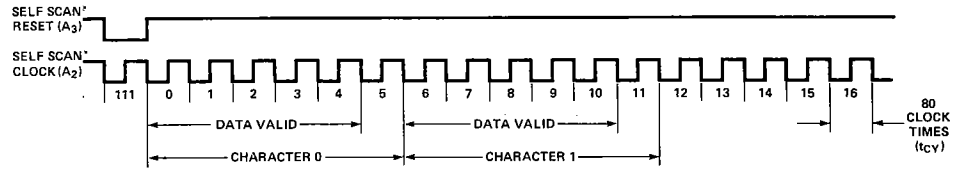


Figure 17. Gas Discharge (Self-Scan®) Mode Timing – 18 Character Mode.