4289
STANDARD MEMORY INTERFACE

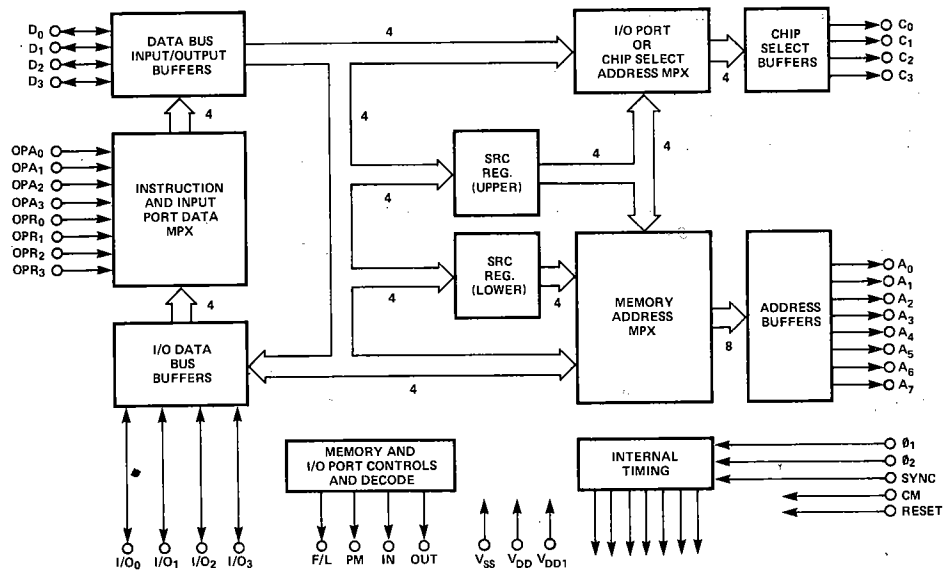
- **Direct Interface to all Standard Memories**
- **Allows Read and Write Program Memory**
- **Single Package Equivalent of 4008/4009**
- **TTL Compatible Address, Chip Select, Program Memory Data Lines**
- **40 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70° C**
- **Also Available With -40° to +85° C Operating Range**

The 4289 standard memory interface and I/O interface enables the CPU devices to utilize standard memory components as program data memory. Notably, PROMs (4702A), RAMs (2102) and ROMs can be arranged in a memory array to facilitate system development. Programs generated using the 4289 interface can be committed to MCS-40™ ROMs (4308 and 4001) with no change to software.

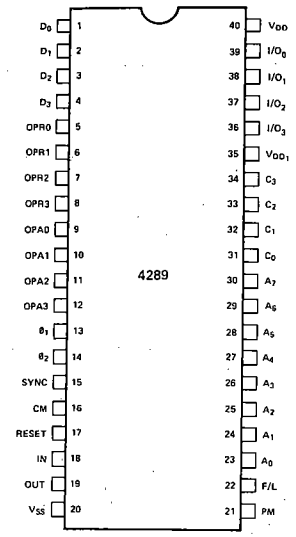
The 4289 also contains a 4 bit bi-directional I/O port and necessary steering logic to multiplex a host of I/O sources to the CPU. The Read and Write Program Memory instruction allows the user to store data and modify program memory. The device directly addresses 4K of program memory. The address is obtained sequentially during A_1-A_3 states of an instruction cycle. The eight bit instruction is presented to the CPU during M_1 and M_2 states of the instruction cycle via the four bit data bus.

The 4289 stores the SRC instruction operand as an I/O address and responds to the ROM I/O instructions (WRR and RDR) by reading or writing data to and from the processor and 4289 I/O bus.

BLOCK DIAGRAM



PIN CONFIGURATION



Pin Description

Pin No.	Designation/ Type of Logic	Description of Function
1-4	D_0-D_3/Neg.	Bidirectional data bus. All address, instruction and data communication between processor and the PROGRAM MEMORY or I/O ports is transmitted on these 4 pins.
5-8	OPR_0-OPR_3/Pos.	The high order 4 bits (OPR) of the instruction or data (RPM) from the PROGRAM MEMORY are transferred to the 4289 on these pins.
9-12	OPA_0-OPA_3/Pos.	The low order 4 bits (OPA) of the instruction or data (RPM) are transferred to the 4289 on these pins.
13-14	ϕ_1-ϕ_2/Neg.	Non-overlapping clock signals which are used to generate the basic chip timing.
15	SYNC/Neg.	Synchronization input signal driven by SYNC output of processor.
16	CM/Neg.	Command input driven by CM-ROM output of processor. Used for decoding SRC and I/O instructions.
17	RESET/Neg.	RESET input. A negative logic "1" level (V_{DD}) applied to this input resets the FIRST/LAST flip-flop.
18	IN/Neg.	Output signal, active low (V_{DD}), generated by the 4289 when the processor executes an RDR or RPM instruction.
19	OUT/Neg.	Output signal, active low (V_{DD}), generated by the 4289 when the processor executes a WRR or WPM instruction.
20	V_{SS}	Most positive supply voltage.
21	PM/Neg.	Output signal, active low (V_{DD}), generated by the 4289 when the processor executes an RPM or WPM instruction.
22	F/L/Neg.	Output signal generated by the 4289 to indicate which half-byte of PROGRAM MEMORY is to be operated on (V_{DD} = OPR, V_{SS} = OPA).
23-30	A_0-A_7/Pos.	Address output buffers. The demultiplexed address values generated by the 4289 from the address data supplied by the processor at A_1 and A_2.
31-34	C_0-C_3/Pos.	Chip select output buffers. The address data generated by the processor at A_3 or during an SRC are transferred here.
35	V_{DD1}	Supply voltage for address and chip select buffers.
36-39	I/O_3-I/O_0/Pos.	Bidirectional I/O data port. Data to and from I/O devices or data to write PROGRAM MEMORY are transferred via these pins.
40	V_{DD}	Main power supply pin. Value must be V_{SS} - 15V ± 5%.

Functional Description

The 4289 enables the 4 bit CPU chip (4004 or 4040) to interface to standard memory components. This allows construction of prototype or small volume systems using electrically programmable ROMs or RAMs in place of 4001 or 4308 mask programmable ROMs. Since 4001s or 4308s also contain up to 16 mask programmable I/O ports, the 4289 has provisions for directly addressing 16 channels of 4 bit I/O ports. In its role as a Memory and I/O interface device, the 4289 provides three different types of operation, namely:

a. Interface to Program Memory for instruction fetch operations.
b. Interface to Input/Output ports for storing or fetching data using WRR, RDR instruction.
c. Interface to R/W Program Memory for program alteration using WPM, RPM instructions. This feature may also be used for storing or fetching data, thus allowing the use of standard R/W RAM for data storage via the 4289.

These three basic operations will be discussed in detail in the following paragraphs.

Instruction Execution

The contents of the data bus at A_1, A_2, and A_3 are latched by the 4289 and transferred to the address and chip select output buffers. The low order address at A_1 is transferred to A_0-A_3 outputs, the middle order address at A_2 is transferred to A_4-A_7 outputs and the high order address at A_3 is transferred to C_0-C_3 outputs. These 12 output lines provide the necessary address and chip select signals to interface to a 4K x 8 bit Program Memory.

The 8 bit word selected by A_0-A_7 and C_0-C_3 is transferred to the processor via the OPR_{0-3}, OPA_{0-3} input lines and the data output buffer. The high order bits (OPR) are transferred at M_1 and the low order 4 bits (OPA) are transferred at M_2.

The 4289 has been designed to work equally well with either the 4004 or 4040 processor elements. Since the 4040 is provided with two CM-ROM controls which allow it to directly address up to 8K x 8 bits of Program Memory (4K x 8 bits selected by each CM-ROM control), two 4289s would be required for full memory capability. In this case, one 4289 would be controlled by CM-ROM0 and the other by CM-ROM1. The 4289 which receives CM at A3 would be enabled to transfer data at M_1 and M_2.

It should be noted that the two CM-ROM controls permit the simultaneous use of 4001, 4308, and 4289 in the same system. The ROM's 4001 and 4308 can be mixed and assigned to one CM-ROM control line while a single 4289 can be assigned to the other. However, within one CM-ROM control line, 4289, 4001, and 4308 cannot be mixed, since the 4289 does respond to a full 4K of memory by its design and thus would overlap program memory address with the 4001 or 4308.

I/O Port Operation

When the processor executes an I/O port instruction (WRR or RDR), a previously selected I/O port (via an SRC instruction) is enabled to receive or transmit 4 bits of data. In the case of WRR, the selected output port receives the 4 bit contents of the processor accumulator, and in the case of RDR, the selected input port transmits 4 bits of data to the processor accumulator. The 4 bit value sent out at X_2 time of the SRC instruction is used as the port address. Since the 4289 is capable of addressing 16 4 bit I/O ports, it must therefore be capable of storing the SRC address sent by the processor and presenting that address to the external I/O port selection logic for WRR or RDR instructions which follow. To accomplish this, the 4289 behaves as follows:

a. When the processor executes an SRC instruction, the 4289 stores the address sent out by the processor at X_2 and X_3. The contents of the upper 4-bits of the SRC register are transferred during every X_1 time to the chip select lines and are available for subsequent I/O instructions' port selection.
b. When the processor then executes a WRR instruction, the 4289 latches the data sent out by the processor at X_2 and transfers this data to the I/O output buffer. This buffer is enabled during X_3 and transmits the data to the selected output port. So that external port logic may be enabled to receive the data, the 4289 generates the OUT strobe signal.
c. When the processor executes an RDR instruction, the 4289 generates the IN strobe. This enables the selected input port to transmit its data to the I/O bus, where it is latched by the 4289 and transferred to the processor at X_2.

Note that in a system using ROMs, the 4 bit port number is decoded by the ROM chip itself. Where a 4289 is used, the 4 bit port number outputted at the chip select lines C_0-C_3 must be externally decoded to select the appropriate I/O device.

Read/Write Program Memory Operations

If the 4289 is used in conjunction with the 4040, both the WRITE and READ PROGRAM MEMORY (WPM/RPM) functions are directly available (only the WPM is available for 4004 systems). To accomplish these operations, the following are required:

a. A program memory address.
b. The proper control signals.
c. A means of transmitting the data to be stored or fetched.

The 4289 provides all of these as described below.

Program Memory Address

The address for an RPM or WPM operation is provided by the 8 bit contents of the SRC register. Note that the RPM or WPM instruction must have been preceded by an SRC instruction which loaded an 8-bit address into the 4289's SRC register. This 8-bit address is the full address of an 8-bit word in one Read/Write Program Memory page (256 bytes). If more than one page of Read/Write Program Memory is desired, these pages must be selected by external logic controlled via other output ports of the system. At X_1 of every instruction cycle the 8 bit value contained in the SRC register is transferred to the address output buffers A_0-A_7. This address will select 1 out of 256 program memory words.

During execution of WPM or RPM, the 4289 does not transfer the high order 4 bits of the SRC register to C_0-C_3.

Instead, it forces all 4 chip select output buffers to a logic "1" state (positive true logic or V_{SS}). This forcing of C_0-C_3 to all "1s" can be used to indicate the execution of a WPM or RPM instruction. The PM output signal is also generated whenever a proper memory operation (WPM or RPM) is being performed. If only one page of R/W memory is required, the 1111 condition on C_0-C_3 or the PM signal can be used to enable that page. If more than one page is required, an additional output port of the system along with external logic will be necessary to provide the 1 out of 16 page select function.

Since the program memory is organized as 8 bit words, and since RPM and WPM are transmitting only 4 bit words, it is also necessary to specify either the upper or lower half-byte of program memory.

This is done automatically by a FIRST/LAST flip-flop and output signal in the 4289. The state of this flip-flop is used to generate the control signal F/L which determines the proper half-byte of program memory. If F/L is a logic "1" state (V_{DD}), OPR is selected. When F/L is a logic "0" (V_{SS}), OPA is selected. The user can directly reset the FIRST/LAST flip-flop to logic "0" (V_{SS}) in the 4289 by applying a RESET signal.

Starting from a "reset" condition the FIRST/LAST flip-flop automatically toggles after executing either an RPM or WPM instruction. Hence, odd numbered program memory operations select OPA and even numbered program memory operations select OPR (starting with #1 from reset). Alternate WPM and RPM instructions should be used with care since this can cause an out of sequence with the F/L line.

The OUT strobe signal is generated only during WRR and WPM instructions. Hence, the combination of the PM signal (or C_0-C_3 = 1111) and the OUT signal can be used as a WRITE ENABLE for R/W program memory.

Program Memory Data Paths

When the processor executes the WPM instruction, the 4289 latches the data sent out at X_2 by the processor and transfers it via the I/O output buffers to the I/O port. The I/O port must be connected to the data input pins of the R/W memory chips. (Refer to Figure 2 which follows.)

If the processor (4040) executes the RPM instruction, then the entire 8 bit program memory word is transferred to the OPR_0-OPR_3 and OPA_0-OPA_3 inputs of the 4289. Depending on the state of the F/L signal, either the OPA or the OPR half-byte is automatically selected by the 4289.

Data Storage

If Read/Write Memory is interfaced to a 4289 and is used for data storage only, the data is accessed via the WPM and RPM instructions just as Read/Write Program Memory would be accessed. The only difference that the chip select lines C_0-C_3 are never used to select the Read/Write Memory in an instruction fetch operation. The PM pulse would be used to select the Read/Write data memory.

Note that the RAM instructions RDM, WRM, WR0-WR3, RD0-RD3, SBM and ADM cannot be used to access this type of data Read/Write memory.

4008/4009 and 4289 Differences

The functional differences between a 4289 and a 4008/4009 Standard Memory Interface component pair are as follows:

1. The PM pulse of the 4289 (negative logic) is inverted in comparison with the W pulse of the 4008 (positive logic).
2. The W pulse of the 4008 begins in X2 and ends in X3. The 4289's PM pulse begins in X1 and ends in A1.
3. The OUT strobe of the 4289 goes to logical 1 (V_{DD}) for the WRR instructions and the WPM instructions. The OUT strobe of the 4009 goes to logical 1 (V_{DD}) for the WRR instruction only.

4289 Applications

The 4289 can be used to form systems of widely varying complexity. Simple systems containing only one page (256 x 8) of PROGRAM MEMORY and few I/O ports, or more complex systems requiring as many as 32 pages (8K x 8) of memory and 32 I/O ports can readily be implemented. Several examples will be described here.

1. Basic PROM Microcomputer System (Figure 1). This system contains:
   a. 1K x 8 bits of PROGRAM MEMORY (4702A PROM)
   b. 1280 bits of DATA MEMORY (4002 RAM) organized as 16 20-character registers
   c. 4 RAM output ports (4002)
   d. 4 I/O ports.

This system uses a 3205 1 out of 8 decoder to decode the input port addressed by the CPU. Two chip select signals (C_0 and C_1) are combined with the IN signal, which is activated low to indicate an input operation, to select one of four input ports. The 3205 enables one DM 7098 three-state buffer.

In a similar manner, one 3205 and the OUT signal, which is activated to indicate an output operation, are used to select one of four output ports.

2. Standard PROM and RAM Memory System (Figure 2). This system again contains 4 pages of PROM storage but, in addition, has one page of RAM storage which can be used for either PROGRAM or DATA storage by using the WPM/RPM instructions. (The RPM instruction is valid only with the 4040.) The RAM storage has been implemented with two 2101's (256 x 4 static RAM). Notice that separate WRITE ENABLE signals must be generated for the upper and lower half-bytes of RAM.

Note that the inputs to the 2101 RAMs are connected to the 4289 I/O port while their outputs are connected directly to the OPR-OPA lines.

The 2101 RAMs can be chip selected through their active low chip select lines in either of two cases:

1. By an address decode of 4 when the RAMs are addressed as Program Memory for instruction fetch.
2. By the PM signal when addressed as a RAM read or write via an RPM or WPM instruction. For write operations, the TTL logic shown selects one of the

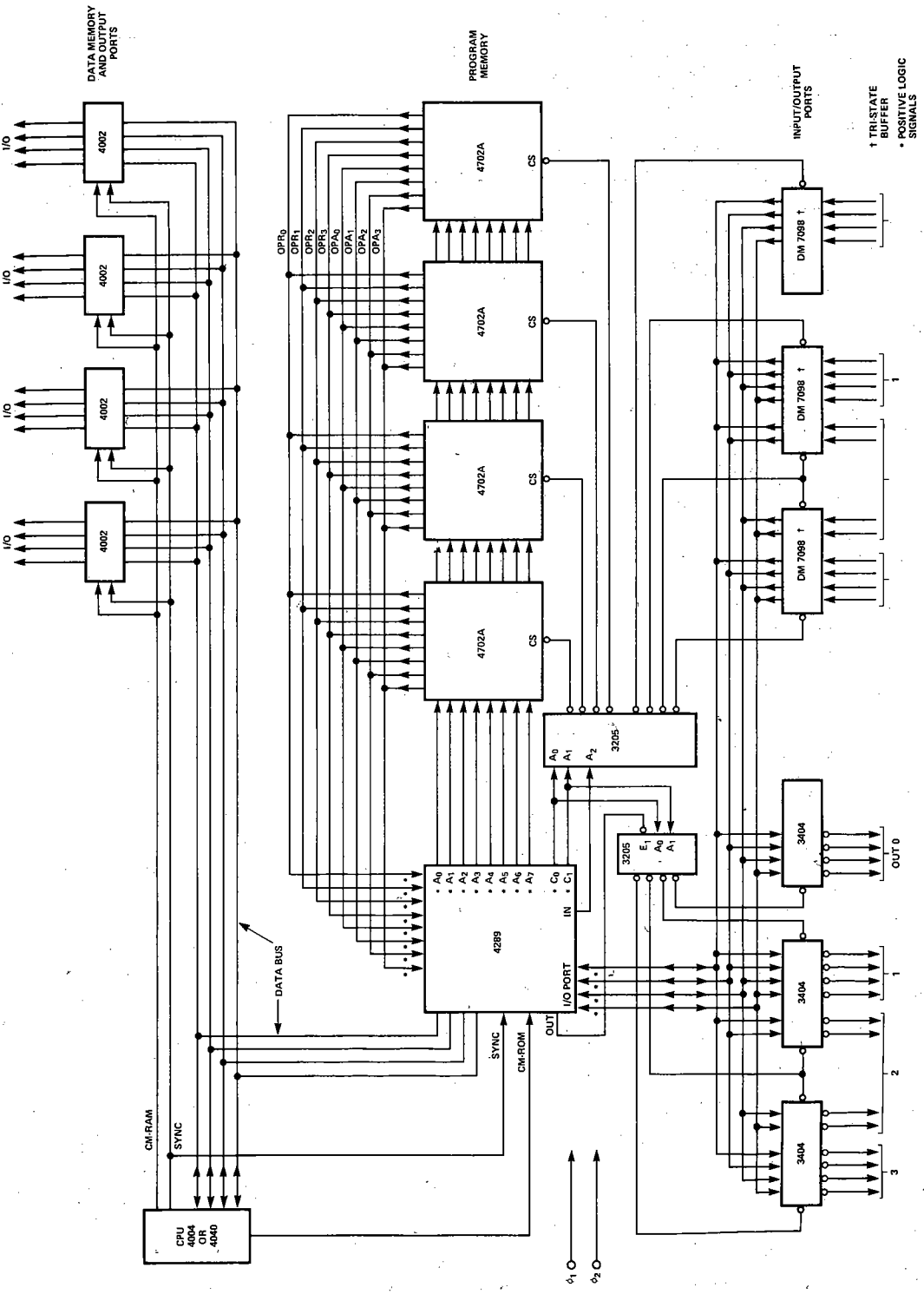


Figure 1. Basic PROM Memory System

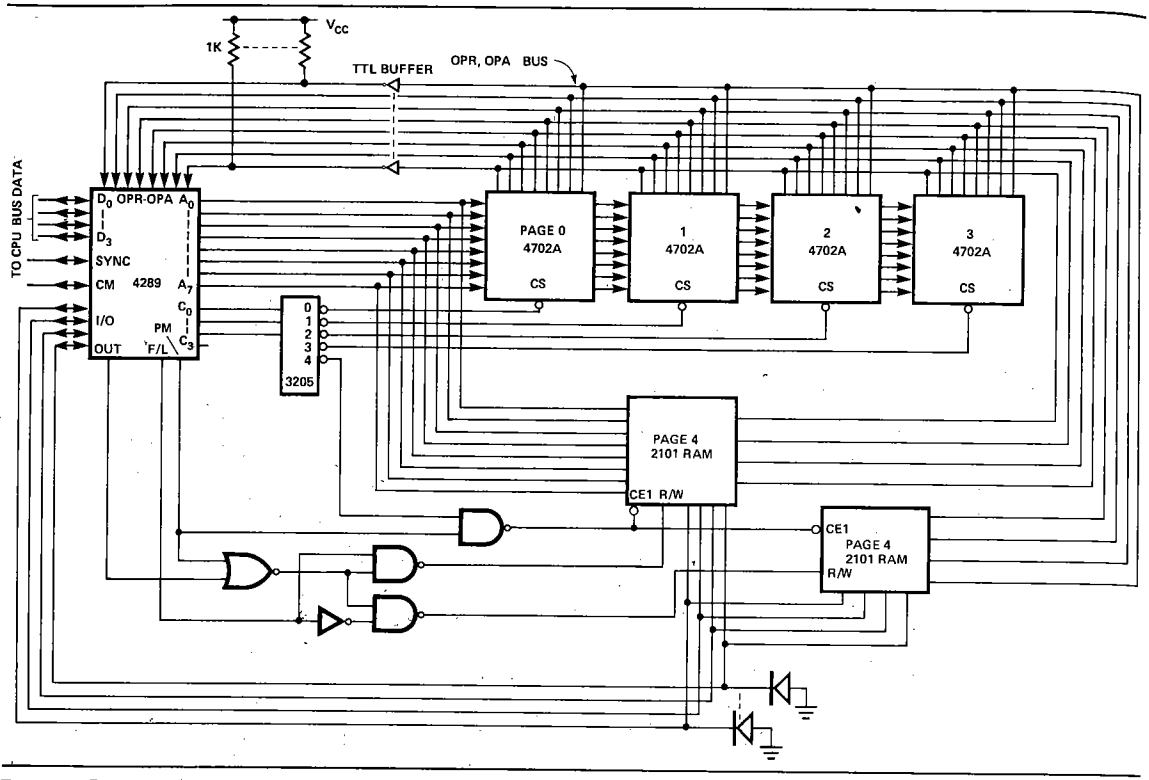


Figure 2. PROM and RAM System.

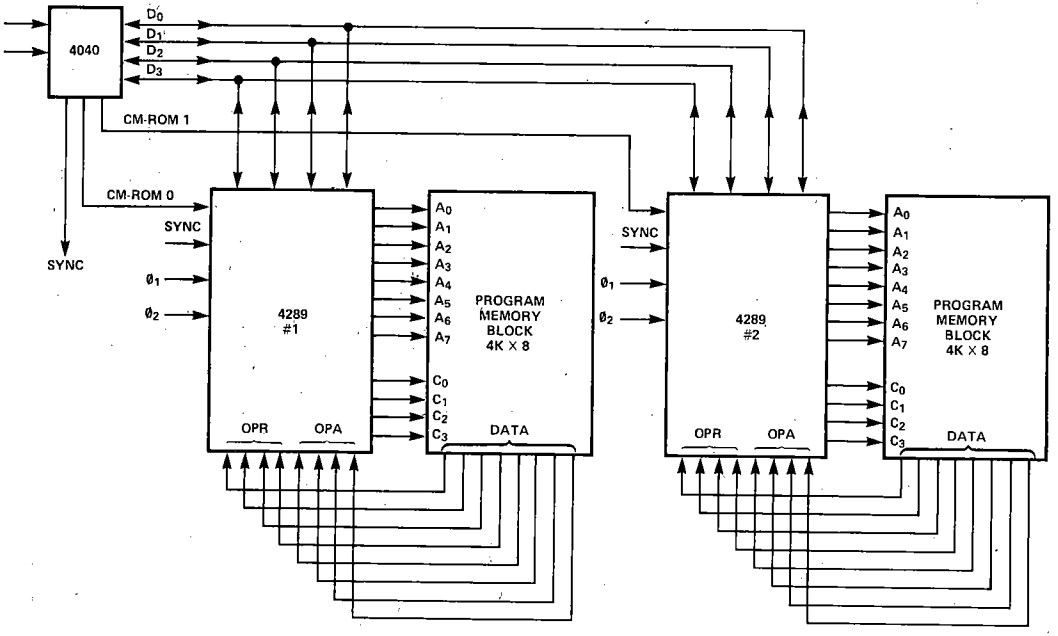


Figure 3. Two Memory Bank System.

two 2101 Read/Write lines according to the F/L signal of the 4289.

The TTL buffers are placed on the data bus to facilitate the compatability between the NMOS RAMs and the PMOS PROMS. The inverters limit the negative excursion of the PROM outputs which may damage the RAMs. The TTL pull-up is required to ensure the V_{IH} threshold level.

3. Two Memory Bank System (Figure 3). Two 4289s are used in this 4040 system giving addressability to a full 8K bytes of PROM memory. In this case each 4289 is controlled from a separate CM-ROM control signal. The CM-ROM$_0$ and CM-ROM$_1$ lines are generated by the 4040. This system cannot be implemented with the 4004.

4289, 4702A System Considerations

1. When utilizing the 4289 with more than six 4702As,a TTL buffer as shown in Figure 4 should be inserted in series with the OPR, OPA lines to achieve maximum clock rate. The buffer may be inverting or non-inverting.

   However, use of a 5.1KΩ resistor on the 4702A output to V_{SS} will allow up to 6 x 4702As to be used without TTL buffers and still achieve maximum clock rate.

2. 4702A access times to meet MCS-40 at $t_{CY} = 1.35\mu$ sec are guaranteed with pure capacitive load of 75pF and with load of 240pF plus a TTL buffer on the 4702A output.

   To operate with more than 6 x 4702A without TTL buffer, the limiting specification is t_{CO} and this increases 5 nsec/pF for capacitance above 75pF; MCS-40 t_{CY} must be increased 2.5ns/pF.

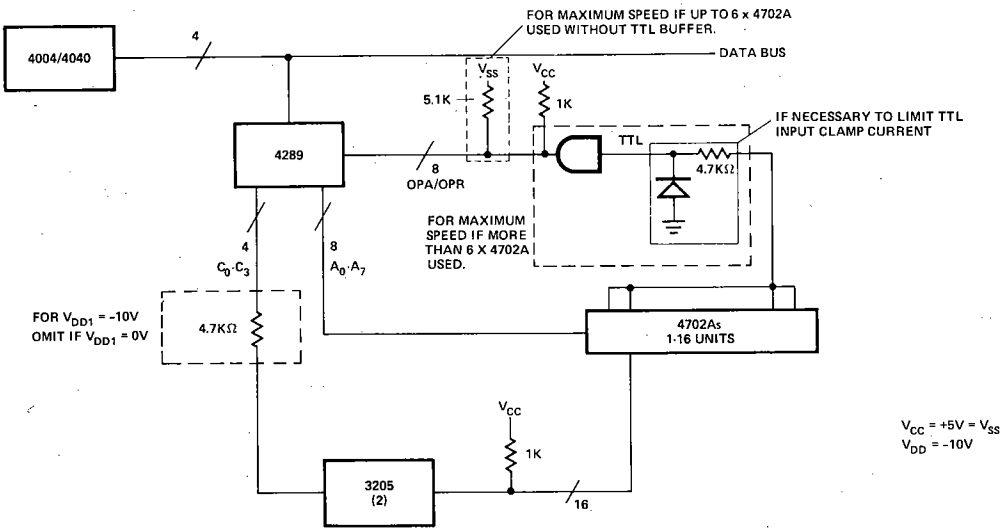


Figure 4. 4289 and 4702A Block Diagram.

Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -55°C to + 125°C
Input Voltages and Supply Voltage
with respect to Vss ..... +0.5V to -20V
Power Dissipation ..... 1.0 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400 nsec; $t_{\phi D2}$ = 150 nsec; 4289 V_{DD1} = V_{SS} -5V. Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless Otherwise Specified.

SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
I_{DD}	Average Supply Current		30	40	mA	T_A = 25°C

INPUT CHARACTERISTICS—ALL INPUTS EXCEPT I/O PINS

I_{LI}	Input Leakage Current			10	μA	V_{IL} = V_{DD}
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{ILO}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	OPR/OPA
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	

OUTPUT CHARACTERISTICS—ALL OUTPUTS EXCEPT I/O PINS

I_{LO}	Data Bus Output Leakage Current			10	μA	V_{OUT} = -12V
V_{OH}	Output High Voltage	V_{SS}-.5V	V_{SS}		V	Capacitive Load
I_{OL}	Data Lines Sinking Current	8	15		mA	V_{OUT} = V_{SS}
I_{OL}[1]	Address Line Sinking Current	7	13		mA	V_{OUT} = V_{SS}, V_{DD1} = V_{DD}
I_{OL}	In, Out, F/L, PM Sinking Current, Chip Select	1.6	4		mA	V_{OUT} = V_{SS} -4.85 V_{DD1} = V_{DD}
V_{OL}[2]	Chip Select Output Low Voltage			V_{DD1}+.5	V	I_{OL} = .4mA
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	V_{SS}-12		V_{SS}-6.5	V	I_{OL} = 0.5mA
R_{OH}	Output Resistance, Data Line "0" Level		150	250	Ω	V_{OUT} = V_{SS} -.5V
R_{OH}	Address, Chip Select Output Resistance, "0" Level		.6	1.2	kΩ	V_{OUT} = V_{SS} -.5V

I/O INPUT CHARACTERISTICS

I_{LI}	Input Leakage Current			10	μA	
V_{IH}[3]	Input High Voltage	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	

I/O OUTPUT CHARACTERISTICS

V_{OH}	Output High Voltage	V_{SS}-.5V			V	I_{OUT} = 0
R_{OH}	I/O Output "0" Resistance		.25	1.0	kΩ	V_{OUT} = V_{SS}-.5
I_{OL}	I/O Output "1" Sink Current	5	12		mA	V_{OUT} = V_{SS} -.5
I_{OL}	I/O Output "1" Sink Current	1.6	4		mA	V_{OUT} = V_{SS} -4.85V
I_{CF}	I/O Output "1" Clamp Current			10	mA	V_{OUT} = V_{SS} -6V

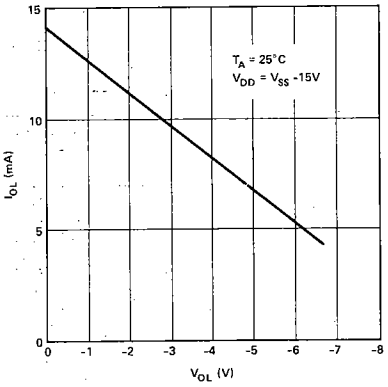
Notes: 1. The address lines will drive a TTL load if a 470Ω resistor is connected in series between the address output and the TTL input.
2. 4289 Address (A_0-A_7) Outputs are also tied to V_{DD1} but are tested with capacitive load only.
3. TTL V_{OH} = 2.4V will ensure 4289 V_{IH} = V_{SS} -1.5V via the 4289 latch. Refer to Figure 5.

D.C. and Operating Characteristics (Continued)

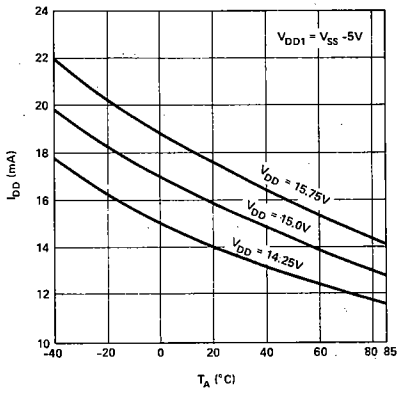
CAPACITANCE

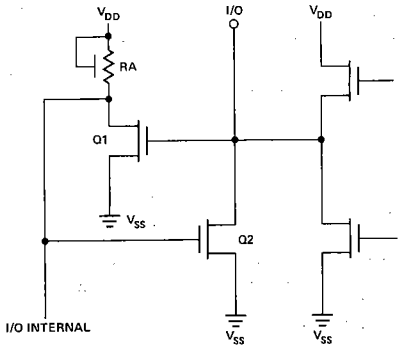
Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
C_ϕ	Clock Capacitance		14	20	pF	$V_{IN} = V_{SS}$
C_{DB}	Data Bus Capacitance		7	10	pF	$V_{IN} = V_{SS}$
C_{IN}	Input Capacitance			15	pF	$V_{IN} = V_{SS}$
C_{OUT}	Output Capacitance			10	pF	$V_{IN} = V_{SS}$

4289 I_{OL} VS. V_{OL} (FOR I/O PINS)



4289 I_{DD} VS. TEMPERATURE





EXPLANATION:

WITH V_{SS} = +5V and V_{DD} = -10V, AN EXTERNAL TTL INPUTTING TO THE 4289 ON THE I/O LINE, RAISES THE I/O LINE TO 2.4V. THE Q1-RA INVERTER TURNS "OFF" AND Q2 PULLS THE I/O LINE TO V_{SS}. A LOW TTL SIGNAL OVERRIDES Q2. IF THE TTL OUTPUT GOES TO THE THIRD STATE, THE EXTERNAL I/O LINES REMAIN HIGH THROUGH Q2.

THE PURPOSE OF THIS CIRCUIT IS TO REMOVE RESISTORS TO $V_{CC} = V_{SS}$ ON TTL OUTPUTS, AS R_1 DOES ON 4001/4308 INPUT PORTS.

MCS 4/40

Figure 5. 4289 I/O Latch.

A.C. Characteristics

T_A = 0°C to 70°C, V_{SS} -V_{DD} = 15V ±5%

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit	Test Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t\phi_R$	Clock Rise Time			50	ns	
$t\phi_F$	Clock Fall Time			50	ns	
$t\phi_{PW}$	Clock Width	380		480	ns	
$t\phi_{D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
$t\phi_{D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500pF Data Lines
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT} = 20pF
t_{A1}[4]	ϕ_1 to Output Delay A_1		400	1000	ns	C_L = 250pF; A_0-A_3
t_{TA1}[4]	Data Bus to Output Delay A_1		500	700	ns	C_L = 250pF; A_0-A_3
t_{A2}[4]	ϕ_1 to Output Delay A_2		400	580	ns	C_L = 250pF; A_4-A_7
t_{TA2}[4]	Data Bus to Output Delay A_2		500	700	ns	C_L = 250pF; A_4-A_7
t_{CS}[4,5]	ϕ_1 to Chip Select Output Delay A_3		150	350	ns	C_L = 50pF
t_{TC}[4,5]	Data Bus to Chip Select Output Delay A_3		250	350	ns	C_L = 50pF
t_{WID}	OPR to Data Bus Delay		250	350	ns	C_{OUT} = 20pF, Data Bus
t_{SRC}	Output Delay at X_1 Time		400	700	ns	C_L = 250pF
t_{S1}	IN Strobe Delay Time			500	ns	C_L = 50pF
t_{S2}	OUT Strobe Delay Time, Falling			500	ns	C_L = 50pF
t_{FD}	F/L and PM Delay Time		300	500	ns	C_L = 100pF
$t_{W,I/O}$	I/O Input Write Time	400	250		ns	
$t_{H,I/O}$	I/O Input Hold Time	40	0		ns	
$t_{D,I/O}$	I/O Output Delay Time		400	1000	ns	C_L = 300pF
t_{WI}	Data In Write Time	350			ns	C_{OUT} = 200pF, Data Bus

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.
2. T_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.
3. All MCS-40 components which may transmit instruction or data to 4004/4040 at M_2 and X_2 always enter a float state until the 4004/4040 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.
4. t_{A1}, t_{A2}, t_{CS} apply if Data Bus is valid before ϕ_1 trailing edge. t_{TA}, t_{TC} apply if Data Bus becomes valid after ϕ_1 trailing edge.
5. Measured at output of 3205 decoder.

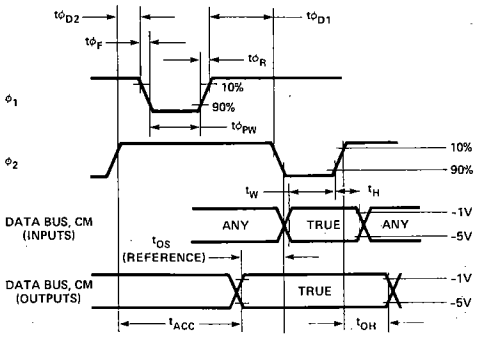


Figure 6. MCS-40 Timing Detail.

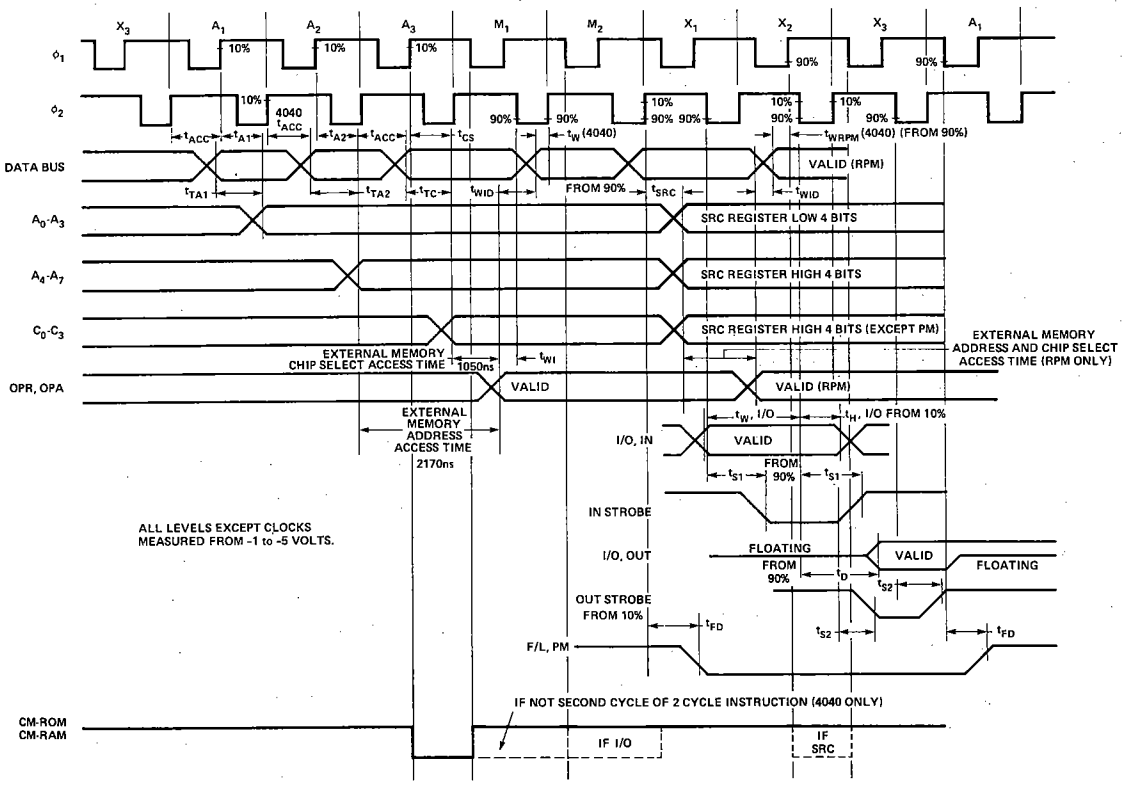


Figure 7. MCS-40 Timing Diagram for 4289.