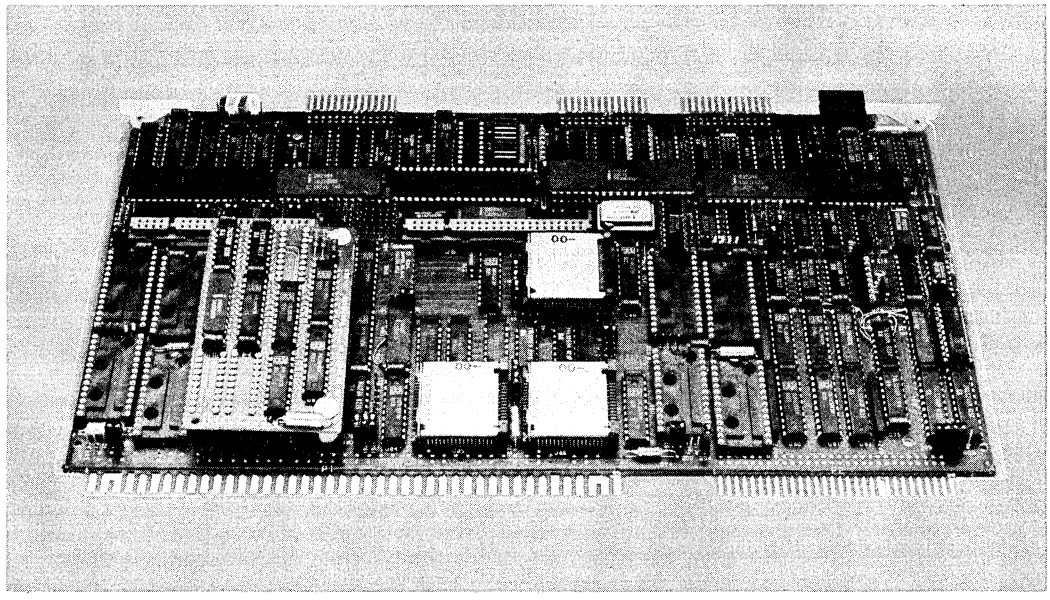
iSBC® 286/10 SINGLE BOARD COMPUTER

- iAPX 286/10 (80286) Microprocessor with 6.0 MHz CPU clock
- Optional 80287 Numeric Data Processor
- iLBX™ (Local Bus Extension) interface for high-speed memory expansion
- Two iSBX™ bus interface connectors for I/O expansion
- Eight JEDEC 28-pin sites for optional RAM/iRAM/EPROM/E^{2}PROM components
- Optional expansion to twelve JEDEC 28-pin sites with an iSBC® 341 28-pin site expansion board
- 16 levels of vectored interrupt control
- Centronics-compatible parallel I/O printer interface
- Two programmable multiprotocol synchronous/asynchronous serial interfaces; one RS232C, the other RS232C or RS422 compatible
- MULTIBUS® interface for multimaster configurations and system expansion

The iSBC® 286/10 Single Board Computer is a member of Intel's complete line of microcomputer modules and systems which take advantage of Intel's VLSI technology to provide economical, off-the-shelf, computer-based solutions for OEM applications. The board is a complete microcomputer system on a 6.75 x 12.0 inch printed circuit card. The CPU, system clock, memory sockets, I/O ports and drivers, serial communications interface, priority interrupt logic and programmable timers, all reside on the board. The iSBC 286/10 board is the first single board computer to incorporate the iAPX 286 CPU and the iLBX™ bus extension. This combination provides the highest performance 16-bit microcomputer system solution. The iLBX architectural expansion maintains this high performance for applications requiring vast amounts of system memory.



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FUNCTIONAL DESCRIPTION

Overview

The iSBC 286/10 board utilizes the powerful iAPX 286 CPU within the MULTIBUS system architecture, enhanced by the iLBX bus, to provide a high performance 16-bit solution. This board also includes on-board interrupt, memory and I/O features facilitating a complete single board computer system.

Central Processing Unit

The central processor for the iSBC 286/10 board is the 80286 CPU operating at a 6.0 MHz clock rate. The 80286 CPU is upwardly compatible with Intel's iAPX 88 and iAPX 86 CPUs. The 80286 CPU runs iAPX 88 and 86 code at substantially higher speeds due to a parallel chip architecture. In addition, the 80286 CPU provides on chip memory management and protection and virtual memory addressing of up to 1 gigabyte per task. Numeric processing power may be enhanced with the optional 80287 numerics processor. The clock rates for the 80286 and the 80287 are independent with the 80287 rate jumper selectable at either 4.0 or 8.0 MHz.

Instruction Set

The 80286 instruction repertoire includes variable length instruction format (including double operand instructions), 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions.

For enhanced numerics processing capability, the 80287 Numeric Data Processor extends the 80286 architecture and data set. Over 60 numeric instructions offer arithmetic, trigonometric, transcendental, logarithmic and exponential instructions. Supported data types include 16-, 32-, and 64-bit integer, 32- and 64-bit floating point, 18-digit packed BCD and 80-bit temporary. The 80287 meets the proposed IEEE P754 standard for numeric data processing and maintains compatibility with 8087-based systems.

Architectural Features

The iAPX 86, 88, 186, and 286 CPU family all contain the same basic set of registers, instructions, and addressing modes. The 80286 processor is upward compatible with the 8086, 8088 and 80186 CPUs.

The 80286 operates in two modes: iAPX 86 real address mode and protected virtual address mode. In iAPX 86

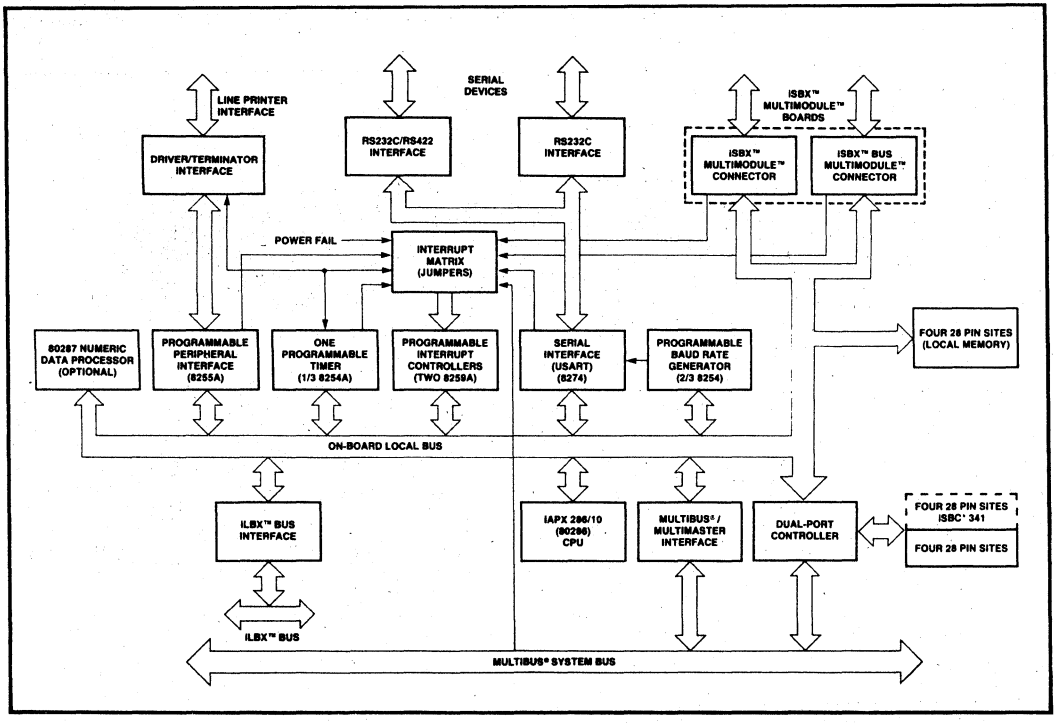

Figure 1. iSBC® 286/10 Block Diagram

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real address mode, programs use real addresses with up to one megabyte of address space. Programs use virtual addresses in protected virtual address mode, also called protected mode. In protected mode, the 80286 CPU automatically maps 1 gigabyte of virtual addresses per task into a 16 megabyte real address space. This mode also provides memory protection to isolate the operating system and ensure privacy of each tasks' programs and data. Both modes provide the same base instruction set, registers, and addressing modes.

VECTORED INTERRUPT CONTROL

Incoming interrupts are handled by two on-board 8259A programmable interrupt controllers and by the 80286's NMI line. Interrupts originating from up to 16 sources are prioritized and then sent to the CPU as a vector address. Further interrupt capability is available through bus vectored interrupts where slave 8259 interrupt controllers resident on separate SBC boards and are cascaded into the on-board interrupt control.

INTERRUPT SOURCES

Twenty-three potential interrupt sources are routed to the interrupt jumper matrix where the user can connect the desired interrupt sources to specific interrupt levels. Table 1 includes a list of devices and functions supported by interrupts.

MEMORY CAPABILITIES

There are eight 28-pin JEDEC sites on-board which may contain a combination of byte-wide devices including RAM, iRAM, EPROM, and E^2PROM. These sites are organized into two 4-site blocks, one of which may be dual-ported. The dual port block may be extended to eight sites (i.e. 12 sites total) by the addition of an iSBC 341 JEDEC site expansion module. The on-board EPROM capacity using twelve 27128 EPROMs is 192 Kbytes. The on-board RAM using ten 8K x 8 RAMs is 80 Kbytes.

SERIAL I/O

A two channel serial communications interface using Intel's 8274 Multi-Protocol Serial Controller (MPSC) is contained on the iSBC 286/10 board. Two independent software selectable baud rate generators provide the MPSC with all common communication frequencies. The protocol (i.e. asynchronous, IBM bisync, or SDLC/HDLC), data format, control character format, parity and baud rate are all under program control. Software interfacing to the MPSC can be via either a polled or interrupt driven routine. One channel may be configured for an RS232C or RS422 interface with the other channel RS232C only. The data, command and signal ground lines for each channel are brought out to two 26-pin connectors.

Table 1. Interrupt Request Sources

Device	Function	Number of Interrupts
MULTIBUS® interface	Requests from MULTIBUS® resident peripherals or other CPU boards	8*
8259A programmable interrupt controller	8 level vectored interrupt request cascaded to master 8259A	1
8274 serial controller	8 level vectored interrupt request cascaded to master 8259A	1
8255A line printer interface	Signals output buffer empty	1
8254 timers	Timer 0, 1 outputs; function determined by timer mode	2
iSBX™ connectors	Function determined by iSBX™ MULTIMODULE™ board	4 (2 per iSBX™ connector)
Bus fail safe timer	Indicates addressed MULTIBUS® resident device has not responded to command within 6 msec	1
Power fail interrupt	Indicates AC power is not within tolerance	1
External interrupt	General purpose interrupt from auxiliary connector, commonly used as front panel interrupt	1
On-board logic	Conditioned interrupt source from edge sense latch, inverter, or OR gate	3

* May be expanded to 56 with slave 8259A PICs on MULTIBUS® boards

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PROGRAMMABLE TIMERS

The iSBC 286/10 board provides three independent, fully programmable 16-bit interval timers/event counters utilizing the Intel 8254 Programmable Interval Timer. Each counter is capable of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs of these counters is jumper selectable. The outputs may be independently routed to the 8259A Programmable Interrupt Controller or to the 8274 MPSC to count external events or provide baud rate generation. The third interval timer in the 8254 is dedicated to providing a clock for the programmable baud rate generator in the iSBC 286/10 board's MPSC serial controller. The system software configures each timer independently to select the desired function. Seven functions are available as shown in Table 2. The contents of each counter may be read at any time during system operation.

Table 2. Programmable Timer Functions

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable one-shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-wave rate generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware triggered strobe	Output goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable.
Event counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counter "window" has been enabled or an interrupt may be generated after N events occur in the system.

LINE PRINTER INTERFACE

An 8255A Programmable Peripheral Interface (PPI) provides a line printer interface, several on-board functions, and four non-dedicated input bits. Drivers are provided for a complete Centronics compatible line printer interface. The on-board functions implemented with the PPI are power fail sense, override, NMI mask, non-volatile RAM enable, clear timeout interrupt, LED 0 and 1, clear edge sense flop, MULTIBUS interrupt, and serial channel A loopback. The PPI's I/O lines are divided into three eight bit ports: A, B and C. Four non-dedicated input bits allow the state of four user configured jumper connections to be input. The PPI must be programmed for mode 0 with ports A and C used as outputs and port B as input. A "dummy" write to port B is used to set the iSBC 286/10 board to protected mode. The parallel port bit assignment is shown in Table 3.

Table 3. Parallel Port Bit Assignment

Port A — Output	
Bit	**Function**
0	Line Printer Data Bit 0
1	Line Printer Data Bit 1
2	Line Printer Data Bit 2
3	Line Printer Data Bit 3
4	Line Printer Data Bit 4
5	Line Printer Data Bit 5
6	Line Printer Data Bit 6
7	Line Printer Data Bit 7
Port B — Input	
Bit	**Function**
0	General Purpose Input 0
1	General Purpose Input 1
2	General Purpose Input 2
3	General Purpose Input 3
4	Line Printer ACK/ (Active Low)
5	Power Fail Sense/ (Active Low)
6	Line Printer Error (Active Hi)
7	Line Printer Busy (Active Hi)
Port C — Output	
Bit	**Function**
0	Line Printer Data Strobe (Active Hi)
1	Override/ (Active Low)
2	NMI Mask (0 = NMI Enabled)
3	Non-Volatile RAM Enable; Clear Timeout Interrupt/
4	LED 0 (1 = On); Clear Edge Sense Flop/
5	MULTIBUS® Interrupt (1 = Active)
6	Serial CHA Loopback (0 = Online, 1 = Loopback)
7	LED 1 (1 = On); Clear Line Printer Ack Flop/

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MULTIBUS® System Architecture

OVERVIEW

The MULTIBUS system architecture includes three bus structures: the system bus, the local bus extension and the MULTIMODULE™ expansion bus as shown in Figure 2. Each bus structure is optimized to satisfy particular system requirements. The system bus provides a basis for general system design including memory and I/O expansion as well as multiprocessing support. The local bus extension alllows large amounts of high performance memory to be accessed from a CPU board over a private bus. The MULTIMODULE extension bus is a means of adding inexpensive I/O functions to a base CPU board. Each of these three bus structures are implemented on the iSBC 286/10 board providing a total system architecture solution.

SYSTEM BUS – IEEE 796

The MULTIBUS system bus is Intel's industry standard, IEEE 796, microcomputer bus structure. Both 8- and 16-bit single board computers are supported on the IEEE 796 structure with 24 address and 16 data lines. In its simplest application, the system bus allows expansion of functions already contained on a single board computer (e.g., memory and digital I/O). However, the IEEE 796 bus also allows very powerful distributed processing configurations with multiple processors and intelligent slave, I/O and peripheral boards capable of solving the most demanding microcomputer applications. The MULTIBUS system bus is supported with a broad array of board level products, LSI interface components, detailed published specifications and application notes.

SYSTEM BUS – EXPANSION CAPABILITIES

Memory and I/O capacity may be expanded and additional functions added using Intel MULTIBUS compatible expansion boards. Memory may be expanded by adding user specified combinations of RAM boards, EPROM boards, or combination boards. Input/output capacity may be added with digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers, or hard disk controllers. Modular expandable backplanes and cardcages are available to support multiboard systems.

SYSTEM BUS – MULTIMASTER CAPABILITIES

For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically sharing system tasks through communication of the system bus), the iSBC 286/10 board provides full system bus arbitration control logic. This control logic allows up to three iSBC

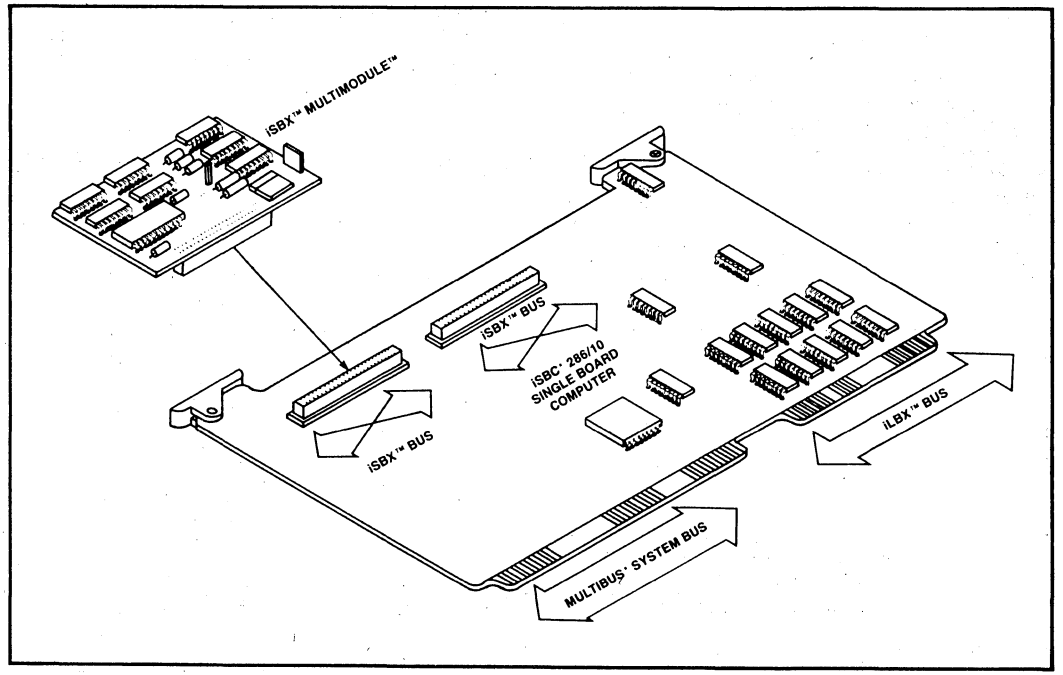

Figure 2. MULTIBUS® System Architecture

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286/10 boards or other bus masters, including iSBC 80 family MULTIBUS compatible 8-bit single board computers to share the system bus using a serial (daisy chain) priority scheme and allows up to 16 masters to share the MULTIBUS system bus with an external parallel priority decoder. In addition to multiprocessing configuration made possible with multimaster capability, it also provides a very efficient mechanism for all forms of DMA (Direct Memory Access) transfers.

iLBX™ BUS – LOCAL BUS EXTENSION

The iSBC 286/10 board also provides the local bus extension (iLBX) of the MULTIBUS architecture. This standard extension allows on-board memory performance with physically off-board memory. The combination of a CPU board and iLBX memory boards is architecturally equivalent to a single board computer and thus can be called a "virtual SBC". The iLBX is implemented over the P2 connector and requires cabling across the virtual SBCs of a system (see Figure 3). Other Intel products which support the iLBX bus include:

iSBC 028CX 128KB iLBX RAM board
iSBC 056CX 256KB iLBX RAM board
iSBC 012CX 512KB iLBX RAM board
iSBC 428 JEDEC 28-PIN SITE board
iSBC 580 MULTICHANNEL™ interface board

iSBX™ BUS MULTIMODULE™ ON-BOARD EXPANSION

Two 8/16-bit iSBX™ MULTIMODULE connectors are provided on the iSBC 286/10 microcomputer board. Through these connectors, additional on-board I/O functions may be added. iSBX MULTIMODULEs optimally support functions provided by VLSI peripheral components such as additional parallel and serial I/O, analog I/O, small mass storage device controllers (e.g., cassettes and floppy disks), and other custom interfaces to meet specific needs. By mounting directly on the single board computer, less interface logic, less power, simpler packaging, higher performance, and lower cost result when compared to other alternatives such as MULTIBUS form factor compatible boards. The iSBX connectors on the iSBC 286/10 board provide all signals necessary to interface to the local on-board bus, including 16 data lines for maximum data transfer rates. iSBX MULTIMODULE boards designed with 8-bit data paths and using the 8-bit iSBX connector are also supported on the iSBC 286/10 microcomputer board. A broad range of iSBX MULTIMODULE options are available from Intel. Custom iSBX modules may also be designed. An iSBX bus interface specification and iSBX connectors are available from Intel.

Software Support

Real time support for the iSBC 286/10 board is provided by Release 6 of the iRMX 86 operating system. Release 6 of the iRMX 86 operating system is an adaption of the iRMX 86 nucleus to operate on the iSBC 286/10 board in real address mode. Release 6 of the iRMX 86 enhances the ICU for configuration support of the board, adds a driver for the on-board 8274 and supports the 80287. Release 6 of iRMX 86 is completely compatible with earlier versions of iRMX 86.

Intel's family of iRMX operating systems provide high-performance, real time, multitasking O.S. support for Intel's single board computers. iRMX employs a highly configurable, modular structure for easy system configuration and expansion. The iRMX family offers a wealth of design facilities and industry standard languages to support fast, easy development.

Interactive multi-user support will be provided by the XENIX[1] operating system. XENIX is a compatible derivative of UNIX[2], System III.

Language support for the iSBC 286/10 boards real address mode includes Intel's ASM 86, PL/M 86, PASCAL and FORTRAN as well as many third party 8086 languages. Language support for virtual address mode

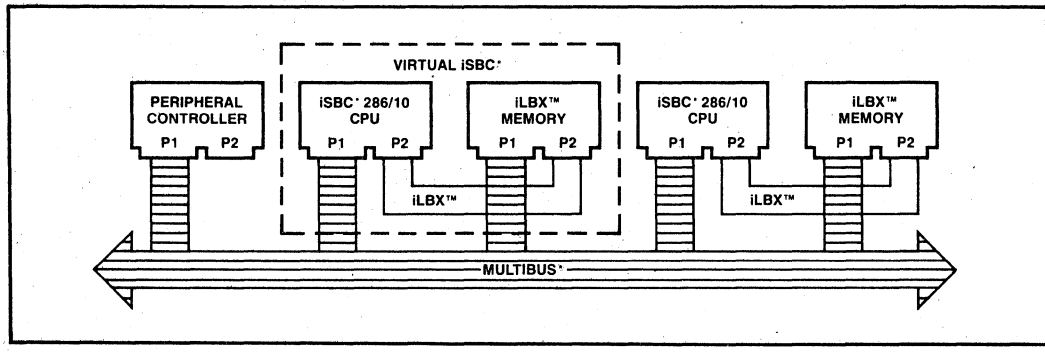

Figure 3. MULTIBUS®/iLBX™ Configuration

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operation includes ASM 286, PL/M 286, PASCAL and C. Programs developed in these languages can be downloaded from an Intel Series III Development System to the iSBC 286/10 board via the iSDM™ 286 System Debug Monitor. The iSDM 286 monitor also provides on-target program debugging support including breakpoint and memory examination features.

[1] Xenix is a trademark of Microsoft Inc.
[2] UNIX is a trademark of Bell Labs.

SPECIFICATIONS

Word Size

Instruction — 8, 16, 24, 32 or 40 bits

Data — 8 or 16 bits

System Clock

CPU — 6.0 MHz

Numeric Processor — 4.0 or 8.0 MHz (Jumper Selectable)

Cycle Time

Basic Instruction — 6.0 MHz - 500 ns; 333 ns (assumes instruction in queue)

NOTE: Basic instruction cycle is defined as the fastest instruction time (i.e. two clock cycles).

Memory Capacity (Maximum)

EPROM — 2716, 8 Kbytes; 2732, 16 Kbytes; 2764, 64 Kbytes; 27128, 128 Kbytes; 27256, 256 Kbytes

E²PROM — 2817A, 16 Kbytes

iRAM — 2186, 16 Kbytes

Static RAM — 8K x 8 devices, 48 Kbytes

NOTES: Two local sites must contain boot-up EPROM or E²PROM. 2716s and 2732s may reside in dual-port sites only. iRAMs may reside in local sites only.

WITH iSBC® 341 MULTIMODULE™

EPROM — 2716, 16 Kbytes; 2732, 32 Kbytes; 2764, 96 Kbytes; 27128, 192 Kbytes; 27256, 256 Kbytes

E²PROM — 2817A, 24 Kbytes

iRAM — 2186, 16 Kbytes

Static RAM — 8K x 8 devices, 80 Kbytes

NOTES: Dual-port sites can address 128 Kbytes of memory maximum. Two local sites must contain boot-up EPROM or E²PROM. 2716s and 2732s may reside in dual-port sites only. iRAMs may reside in local sites only.

I/O Capability

Parallel — Line printer interface, on-board fuctions, and four non-dedicated input bits

Serial — Two programmable channels using one 8274

Timers — Three programmable timers using one 8254

Expansion — Two 8/16-bit iSBX MULTIMODULE connectors

Interrupt Capacity

Potential Interrupt Sources — 23, jumper selectable

Interrupt Levels — 16 vectored requests using two 8259As and the 80286's NMI line.

Serial Communications Characteristics

Synchronous — 5-8 bit characters; internal or HDLC/SDLC character synchronization; automatic sync insertion; even or odd parity.

Asynchronous — 5-8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection; even or odd parity.

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BAUD RATES

Frequency (kHz) (Software Selectable)	Baud Rate (Hz)				
	Synchronous	Asynchronous			
Reference: 1.23 MHz	÷1	÷1	÷6	÷32	÷64
615.	615,000	615,000	38,400	19,200	9,600
307.	307,000	307,000	19,200	9,600	4,800
154.	154,000	154,000	9,600	4,800	2,400
76.8	76,800	76,800	4,800	2,400	1,200
38.4	38,400	38,400	2,400	1,200	600
19.2	19,200	19,200	1,200	600	300
9.6	9,600	9,600	600	300	150
4.8	4,800	4,800	300	150	75
2.4	2,400	2,400	150	75	—
1.2	1,200	1,200	75	—	—
0.6	600	600	—	—	—

TIMERS

Input Frequencies — 1.23 MHz ±0.1% or 3.00 MHz ±0.1% (Jumper Selectable)

OUTPUT FREQUENCIES/TIMING INTERVALS

Function	Single Timer/Counter		Dual Timer/Counter (two timers cascaded)	
	Min	Max	Min	Max
Real-time interrupt	667 ns	53.3 ms	1.33 μs	58.2 min
Programmable one-shot	667 ns	53.3 ms	1.33 μs	58.2 min
Rate generator	18.8 Hz	1.50 MHz	0.000286 Hz	750 kHz
Square-wave rate generator	18.8 Hz	1.50 MHz	0.000286 Hz	750 kHz
Software triggered strobe	667 ns	53.3 ms	1.33 μs	58.2 min
Hardware triggered strobe	667 ns	53.3 ms	1.33 μs	58.2 min
Event counter	—	8.0 MHz	—	—

INTERFACES

MULTIBUS®— All signals TTL compatible

iSBX™ Bus — All signals TTL compatible

iLBX™ Bus — All signals TTL compatible

Serial I/O — Channel A: RS232C/RS422 compatible, configurable as a data set or data terminal; Channel B: RS232C compatible, configured as data set

Timer — All signals TTL compatible

Interrupt Requests — All TTL compatible

CONNECTORS

Interface	Double-Sided Pins (qty.)	Centers (in.)	Mating Connectors
MULTIBUS® System	86	0.156	Viking 3KH43/9AMK12 Wire Wrap
iSBX™ Bus — 8-Bit Data	36	0.1	iSBX™ 960-5
16-Bit Data	44	0.1	iSBX™ 961-5
iLBX™ Bus	60	0.1	Kelam RF30-2803-5 or T&B Ansley A3020 (609-6026 modified)
Parallel I/O	26	0.1	3M 3462-0001 Flat or AMP 88106-1 Flat
Serial I/O	26	0.1	3M 3462-0001 Flat or AMP 88106-1 Flat

MULTIBUS® DRIVERS

Function	Characteristic	Sink Current (mA)
Data	Tri-State	16
Address	Tri-State	16
Commands	Tri-State	32
Bus Control	Open Collector	20

iLBX™ DRIVERS

Function	Characteristic	Sink Current (mA)
Data	Tri-State	9
Address	Tri-State	20
Commands	Tri-State	8
Bus Control	TTL	8

Physical Characteristics

Width — 12.00 in. (30.48 cm)

Height — 6.75 in. (17.15 cm)

Depth — 0.70 in. (1.78 cm)

NOTE: Depth includes a small piggyback on lower left of board.

Weight — 19 oz. (539 gm)

Electrical Characteristics

DC Power Requirements — +5V, 7.0A; +12V, 50 mA; −12V, 50 mA

NOTE: Does not include power for optional EPROM, E^2PROM, or RAM.

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Relative Humidity — to 90% (without condensation)

Reference Manual

145439-001 — iSBC 286/10 Single Board Computer Design Guide (NOT SUPPLIED)

ORDERING INFORMATION

Part Number	Description
SBC 286/10	Single Board Computer