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RGB-GRAPH

VECTOR PLOT 512 x 512 COLOR GRAPHICS DISPLAY CONTROLLER FOR MULTIBUS

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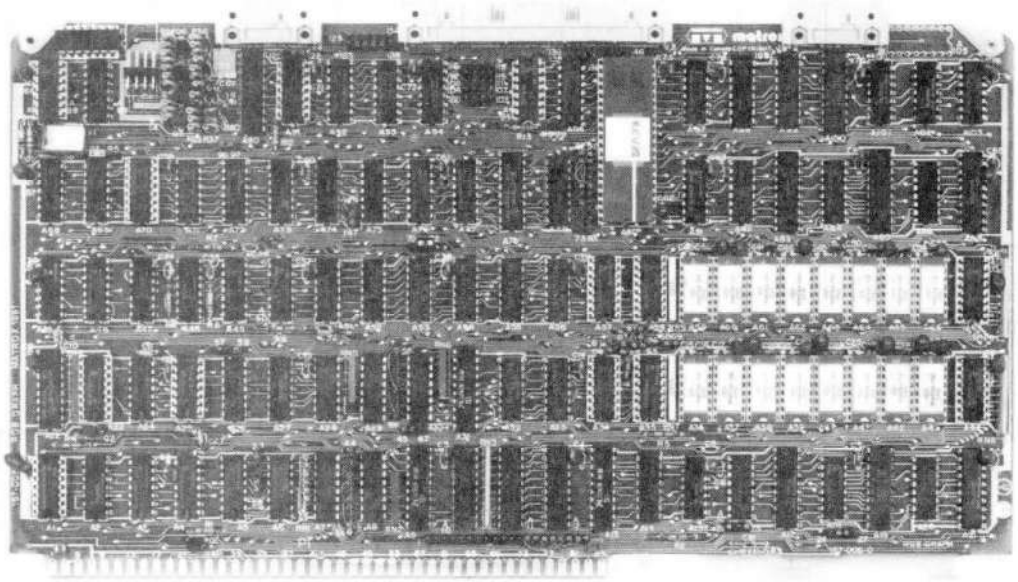
- **512 x 512 pixel resolution standard**
- **4 bits/pixel expandable to 16 bits/pixel**
- **Writing speed of 800ns/pixel**
- **DMA access to video RAM**
- **Light pen interface built-in**
- **Vector plot**
- **Hardware zoom, pan, scroll, and shift, clear, overlay, clipping, video enable**
- **Works with any 8 or 16 bit Multibus* CPU**
- **Add-on RGB-ALPHA board provides color alphanumeric overlay**
- **Add-on VAF-512 board adds:**
  - **— Real-time 512 x 512 frame grabber**
  - **— 16 million color look-up table**
  - **— Hardware vector generator**

The RGB-GRAPH is a member of Matrox's complete line of modular Multibus* compatible color video boards. By using the latest state of the art LSI and VLSI technology, the RGB-GRAPH provides an economical, self-contained solution for OEM color graphics applications requiring high resolution, top performance, and low cost. The board contains advanced video features such as hardware zoom, scroll, shift, pan, clipping, overlay, video masking, etc. which have previously been available only on the most expensive graphics systems at a much higher cost.

Furthermore, the RGB-GRAPH can be combined with other Matrox color video boards such as the color alphanumerics RGB-ALPHA and video processor board VAF-512 (containing real-time 512 x 512 frame grabber, color look-up tables, and a hardware vector generator). The OEM system designer can now easily incorporate powerful tailor-made graphics into his system at a fraction of the cost of a turn-key system.



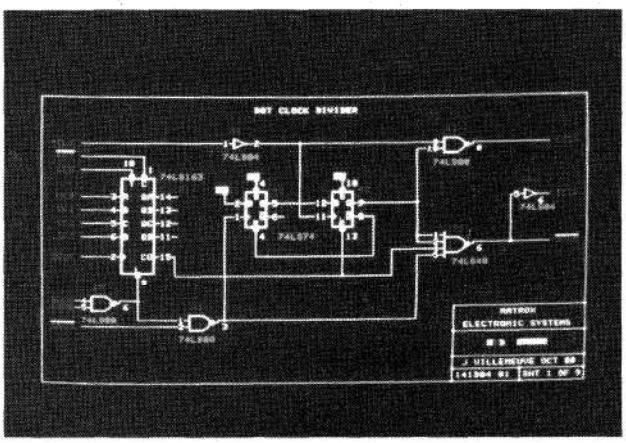


Figure 1. CAD/CAM applications

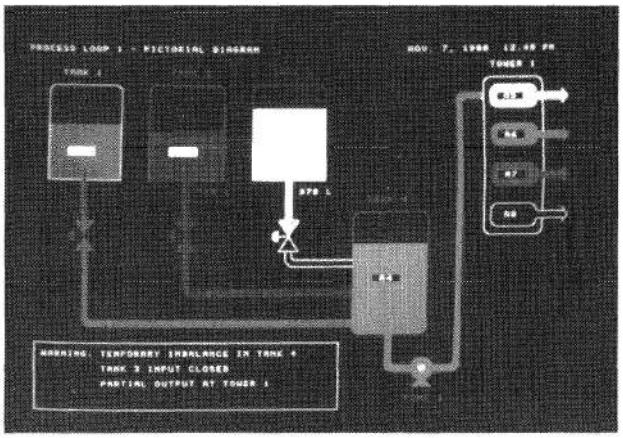


Figure 2. Process Control applications

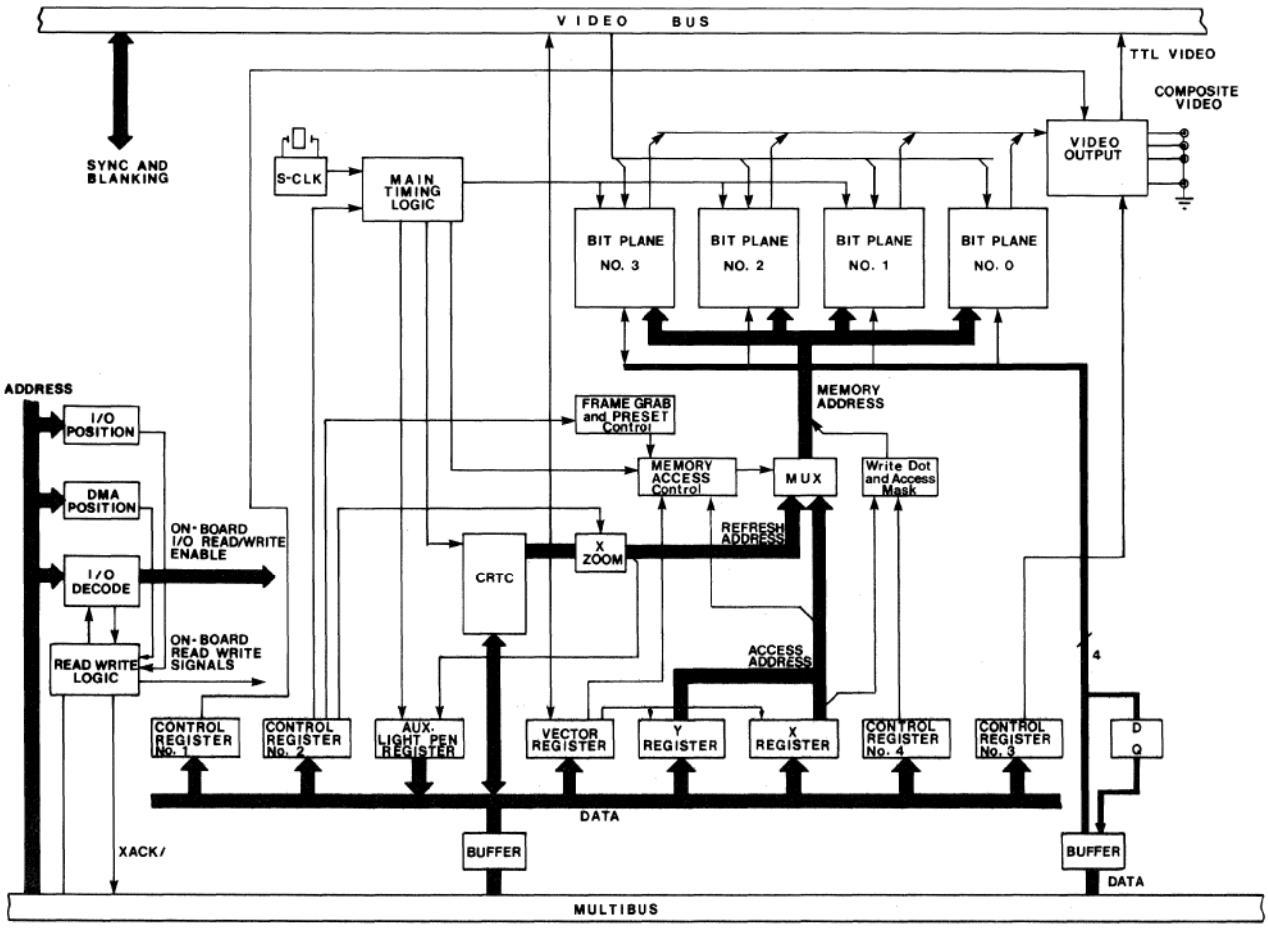


Figure 3. RGB-GRAPH block diagram

RGB-GRAPH FEATURES

Resolution: 512 x 512 or 256 x 256 (special horizontal interlace mode can support 1024 x 512 or 512 x 256)

Bits/Pixel: 1-4 bits/pixel, expandable to 16 bits/pixel with additional RGB-GRAPH boards.

Zoom: Independent X-zoom by 1, 2, 3, 4, 5, 6, 7, 8
Y-zoom by 1, 2, 4
Zoom works on any segment of the 512 x 512 display

Scroll: Up/down scroll (vertical) by multiple of 8 pixels

Shift: Left/right (horizontal) by single or multiple dots

Pan: Scroll and shift can be combined for full two dimensional pan inside the 512 x 512 area

Clipping: 4096 x 4096 addressable area with hardware clip to 512 x 512 for read/write and display

Clear Display: Memory hardware clear to zero (black). All pixels cleared in one frame (33 msec.)

Preset Display: Memory hardware preset to value (color) in data register. All pixels preset in one frame (33 msec.)

Preset Mask: Clear/Preset control of each bit plane by Plane Mask

Video Mask: Video on/off control of each bit plane by VIDEO MASK

Overlay Video: One bit plane video can be combined with the three others for video effects. Functions available are AND, NAND, OR, X-OR

Video Parameters: All video parameters including horizontal and vertical syncs, blanking, frequency, and display format are user software programmable to drive any direct or composite B/W or color CRT monitor

Video Outputs: Direct TTL video (4), composite 75Ω R.G.B. color signals and 16-level grey scale signals are available

Light Pen: Detects true light pen position within one pixel accuracy. Interface built-in

Vector Plot: X-Y registers are auto-increment/decrement

Display RAM: Up to 128K byte on-board memory. CPU can read/write with 400ns (min.) and 1.2 μs (max.) access time/pixel. Memory looks like 262,144 x 4 RAM (single RGB-GRAPH), 262,144 x 16 (four RGB-GRAPHs)

X, Y Pixel Address: Each pixel can be addressed via X, Y registers (12 bits each). Data registers contain pixel color for read/write (I/O addressing)

DMA Pixel Address: 262,144 x 4 (8, 12, 16) display RAM can be accessed in 1K byte blocks (block address in X, Y registers) in DMA mode for image dumping (each pixel is one memory address)

Double Resolution: 512 x 512 x 4 display can be switched to 1024 x 512 x 2 under software control by combining two 512 x 512 x 1 planes. Effectively doubles horizontal resolution

Multibus* Interface: The RGB-GRAPH looks to the user like 16 I/O locations. All communications including pixel read/write, video functions, etc. are accomplished through I/O R/W (no DMA used). With DMA, 1K additional memory space is used.

Access Time: 500ns (max.) for any I/O port; 50ns (min.) — 1.2 μs (max.) for DMA

Video Bus: 50 pin connector provides video inputs and outputs for expanded performance using RGB-ALPHA, VAF-512 and additional RGB-GRAPH boards

ADDITIONAL ADD-ON FEATURES

RGB-ALPHA

Alphanumerics: Color alphanumeric displays can be added by the RGB-ALPHA board (synchronized to the RGB-GRAPH). Formats of up to 132 characters/line and up to 48 lines are user software programmable

RGB-GRAPH

16 Bits/Pixel: By connecting additional RGB-GRAPH boards (max. 4) up to 16 bits/pixel can be obtained (each RGB-GRAPH adds 4 bits/pixel)

VAF-512

Color Look-up: RAM video look-up table increases the number of displayable colors to 2^{24} = 16,772,216. CPU can read/write look-up table

Frame Grabber: Real-time frame grabber digitizes TV camera outputs with 4 or 8 bits/pixel resolution. Spatial resolution is 512 x 512 or 512 x 256. Single frame grab or continuous frame grab under software control

Color Frame Grab: By connecting R.G.B. outputs from a TV camera to the video switcher and grabbing each channel separately, a color picture can be digitized

External Sync: Built-in phase-lock loop synchronizes the RGB-GRAPH to an external composite sync (serrated) for broadcast and mixing applications

Video Switcher: Four-input video switcher enables the user to digitize four separate TV camera inputs under software control

Vector Generator: On-board hardware vector generator with speed of 800ns/pixel. Vector length, slope, and texture are user defined.

ACCESSORIES

CRT Monitors: Matrox supplies a full line of 9" and 14" monochrome monitors, as well as 12", 14", and 19" high resolution (.3 mm pitch) color monitors for interlaced and non-interlaced operations

Light Pen: High speed light pen (LP-600)

SOFTWARE SUPPORT

GRAS-80: Library of high-level graphic primitives (subroutines) including points, vectors, arcs, circles, characters, zoom, scroll, video effects, etc. is available (floppy diskette) in CP/M format. Runs under any Z-80 based CP/M system with the RGB-GRAPH plugged in. Subroutines are accessible from Z-80 assembler or "C".

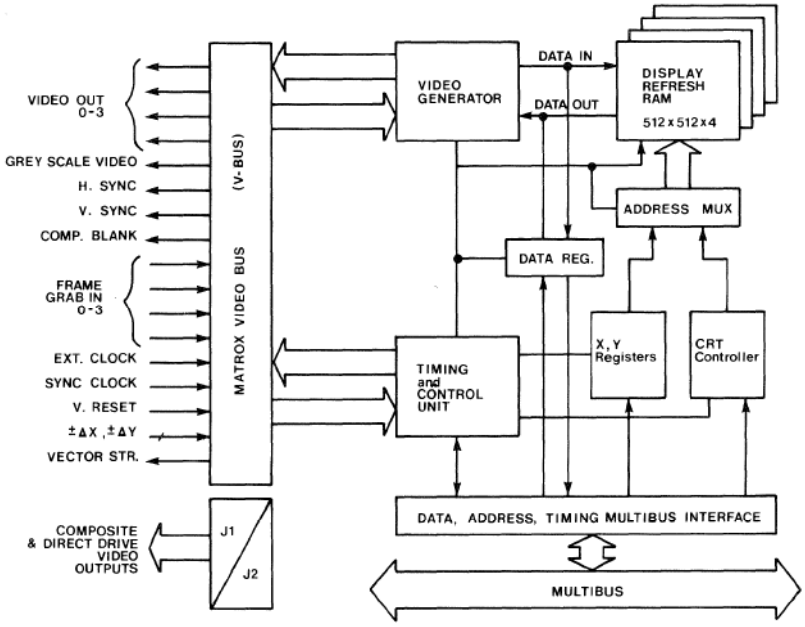


Figure 4. RGB-GRAPH functional blocks

FUNCTIONAL DESCRIPTION

The RGB-GRAPH is a very complex digital graphics system on a single 6.5" x 12" PC board (figure 3). It consists of six main functional blocks (figure 4): CRT Controller, Video Generator, Display RAM, XY Registers, Timing and Control Unit, and Multibus Interface.

The **CRT Controller (CRTC)** is a VLSI IC which provides all video timing signals including horizontal and vertical sync and blanking, display refresh RAM addresses, as well as various other timing and control signals such as cursor, light pen interface, etc. The CRT Controller is software programmable allowing the user to program parameters such as vertical refresh frequency, width and position of horizontal and vertical sync pulses (important when using non-standard CRT monitors), display resolution, etc. To the Multibus CPU, the CRTC appears as an array of 18 registers which are indirectly addressed via two I/O ports.

The **Display Refresh Memory** is made up of 128K bytes of on-board dynamic RAM (for 512 x 512 x 4 resolution) which contains the binary picture information. Each pixel is identified by a unique address in the 262,144 address space (512 x 512). Each address contains 4 data bits which represent the pixel color. The memory is organized as four independent "planes", each containing one data bit (512 x 512 x 1). The display memory can be expanded to 16 planes through the combination of three additional RGB-GRAPH boards.

The CPU can read/write the display RAM in one of two ways. In the XY mode the CPU loads the X and Y registers with the pixel address and then reads/writes the pixel color information through the Data Register. This mode is normally used when drawing graphics point by point. For high speed read/write operations the CPU can access the refresh memory in DMA mode. The display memory is accessed in 1K byte blocks with the starting address of the desired block loaded into the X and Y registers before executing DMA. This mode is usually used when transferring complete images from/to mass storage devices (floppy, Winchester, etc.) or for hard copies.

In addition to the CPU read/write, the display memory is continually scanned by the CRTC every 16.66ms (60 Hz) to generate video signals or, in the frame grabbing mode, to load digitized TV camera images into memory at speeds of over 100 Megabits/second. Memory access arbitration circuitry on the RGB-GRAPH efficiently resolves any contention problems between read/write requests and CRT refresh requests in such a way that the display refresh is "transparent" to the user.

The **X-Y Registers** are 12 bit up/down counter/latches with associated logic containing the address of the pixel being accessed by the graphics cursor (4096 x 4096 addressable area) as shown in figure 5. The CPU can load the X and Y Registers, through programmed I/O, with the pixel's absolute position. Two 8 bit ports are used for each Register. If the contents of either the X or Y Registers exceed the maximum resolution (i.e X > 512, Y > 512) the Clip Circuit will prevent CPU read/write.

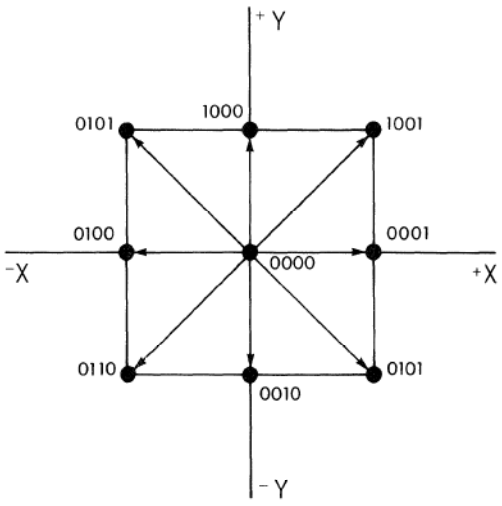


Figure 6. Vector Step Direction

These digital video signals are then passed through double density switches (used for multiplexing two planes to enable the user to double the horizontal resolution, eg. 1024 x 512) and are gated by video mask bits which are stored in the Video Mask Register. The user can, under software control, switch on/off selectively any bit plane enabling a variety of video effects such as animation, multi-page displays, mixing, etc. Overlay logic combines the fourth plane with the other three for various video effects. By plugging the appropriate IC into the overlay socket, the fourth plane can be NANDed (74LS00), ANDed (74LS08), ORed (74LS32), or X-ORed (74LS86) with the other three planes. Video effects such as alphanumerics mixing, multiple windows, graphics cursor, etc. can be accomplished through the use of the overlay feature.

After masking and overlay, the video signals are buffered by high drive buffers (74LS374) with 3-state outputs which are controlled by the video enable signal. The video signals are then placed on the Matrox video bus as TTL video signals (for use by a direct drive TV monitor). The video can alternately be fed to the on-board D/A converter where a composite sync signal is combined with the D/A output to produce a 16 level composite grey scale video signal (75Ω impedance) to drive B/W monitors or hardcopy devices. The TTL level video signals are also combined with a composite sync signal through the composite video buffer to provide composite R,G,B drivers. One of these outputs (normally green) can be intensity controlled by a 2-bit D/A converter connected to planes 2 and 3.

While operating in the frame grabbing mode, the video signals from a TV camera via the VAF-512 board are fed, through a phase lock loop (synchronizes the RGB-GRAPH timing to that of the external sync), to an 8-bit 10 MHz A/D converter. This video signal is then serially input to the 4-bit shift register where it is converted to parallel form and written to the display refresh memory. Note that this is exactly opposite to the generation of video signals during the read operation. Both the read and write video operations are synchronized so that the RGB-GRAPH can operate in a continuous frame grabbing mode (write new pixel data after previous pixel is read).

Various hardware video functions are performed in different sections of the RGB-GRAPH board rather than at one place. Video masking, overlay, D/A conversion, and double density switching are performed in the Video Generator section. Vector plotting and clipping are done through the X, Y Registers, X-zoom, shift, screen clear, and selected plane clear are done in the Timing and Control Unit, and scroll, Y-zoom, user programmable video parameters and light pen interface are handled by the CRT Controller chip.

The **Timing and Control Unit** generates signals for the CRTC as well as all signals required by the display refresh memory (figure 8). It consists of the main oscillator (X-TAL = 10 MHz), variable modulo counters (divide by 1-8) which are controlled by the X-zoom factor to produce the appropriate load and shift signals for the display and a divide by 16 counter which, with a timing PROM, generates a series of timing signals for the memory refresh (RAS, CAS).

The **Multibus* Interface** contains the logic required to interface the RGB-GRAPH to the Multibus*. The RGB-GRAPH looks like 16 consecutive 8-bit wide I/O locations strapped to any 16 address boundary. 8-bit (8085, Z-80A) or 12-bit (8086) I/O addressing can be used. The CPU communicates with the RGB-GRAPH by reading or writing into these I/O registers. The only exception is when the board is used in DMA mode. Then the display memory looks to the CPU like a 1K byte block of RAM (4, 8, 12 or 16 bits wide for 1, 2, 3, or 4 RGB-GRAPH cards). The starting address of the 1K byte block can be positioned anywhere in the 20-bit address space.

DISPLAY SYSTEM CONFIGURATIONS

The Matrox family of advanced color graphics boards; which include the RGB-GRAPH, RGB-ALPHA and VAF-512 offer the OEM system designer the unique capability to design a powerful optimal graphics system with equal or even superior performance to turn-key graphics system, at a lower cost. Futhermore, by using general purpose OEM boards (from Matrox, Intel, NEC, or other suppliers), the user can add CPUs (8 or 16 bit), memory, disk interfaces, etc. Software support, in the form of a graphics primitives library, which runs under CP/M DOS still further simplifies design of the custom graphics systems. Hardware upgrade capabilities enables adding extra display functions by simply plugging in additional boards (more bits/pixel, higher speed, frame grabbing, etc.).

SINGLE BOARD DISPLAY SYSTEM

Using a single RGB-GRAPH board provides for a versatile graphics system that can be used in many display applications from B/W to color.

RESOLUTION	BITS/ PIXEL	PART NUMBER	APPLICATION
256 x 256	1	RGB-G/16/1	Non interlaced B/W or color systems
256 x256	4	RGB-G/16/4	Grey scale or 16 color display system
512 x 256	2	RGB-G/16/4	High res. B/W, one bit for graphics and one bit for alphanumerics
512 x 512	1	RGB-G/64/1	B/W display systems
512 x 512	4	RGB-G/64/4	Grey scale or 16 color display system
1024 x 512	2	RGB-G/64/4	High res. B/W, one bit for graphics and one bit for alphanumerics

Table 1: Examples of display systems using single RGB-GRAPH

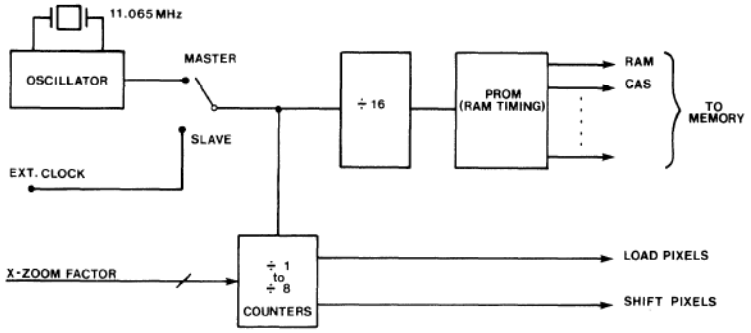


Figure 8. Timing and Control Unit

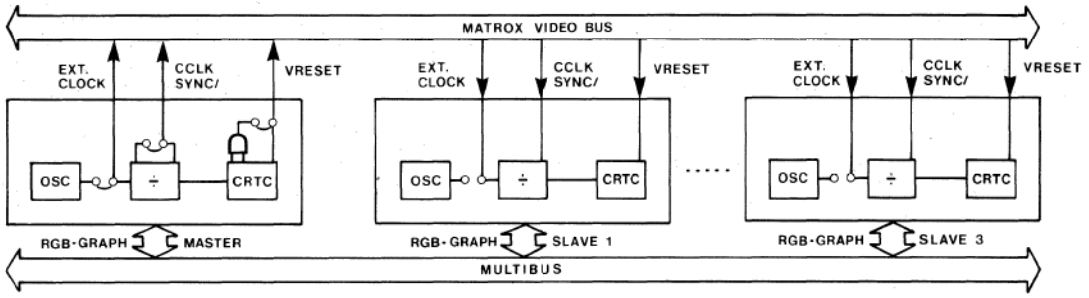


Figure 9. Multiple RGB-GRAPH System

ADDING MORE BITS/PIXEL

Up to four RGB-GRAPH boards can be synchronized together via the video bus (single 50 pin ribbon cable) for up to 16 bits/pixel. Each RGB-GRAPH adds up to 4 bits/pixel.

ADDING ALPHANUMERICS

Alphanumerics can be added to the graphics in three ways. The simplest way is to write alphanumerics, pixel by pixel, from a table stored in RAM or ROM. This offers flexibility in character size, color, position, and font but interferes with the graphics display. The second way is to use one of the bit planes on the RGB-GRAPH exclusively for alphanumerics and overlay it with the graphics planes. The use of a separate alphanumerics board (RGB-ALPHA) offers the highest speed. RGB-GRAPH and RGB-ALPHA are synchronized via the video bus connector. The alphanumeric format (character/line x lines) is user programmable. Video signals can be ORed (on the RGB-ALPHA) or mixed together via a color look-up table (on the VAF-512).

VAF-512

The addition of a VAF-512 board enables the RGB-GRAPH system to digitize a real-time B/W or color video signal from a TV camera or VCR with 4 or 8 bits/pixel. Also, a high speed look-up table on the VAF-512 expands the number of displayable colors to over 16 million. The VAF-512 can also be used for video mixing, animation, etc. A high speed hardware vector generator executes high level graphics commands at 800ns/pixel. The VAF-512 is synchronized via the video bus and it works in 256 x 256, 512 x 256 and 512 x 512 resolution.

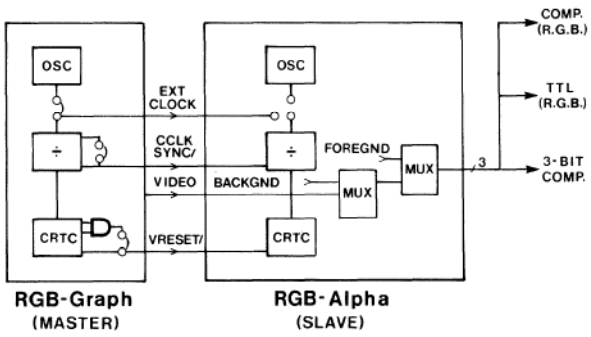


Figure 10. Alphanumerics Overlay

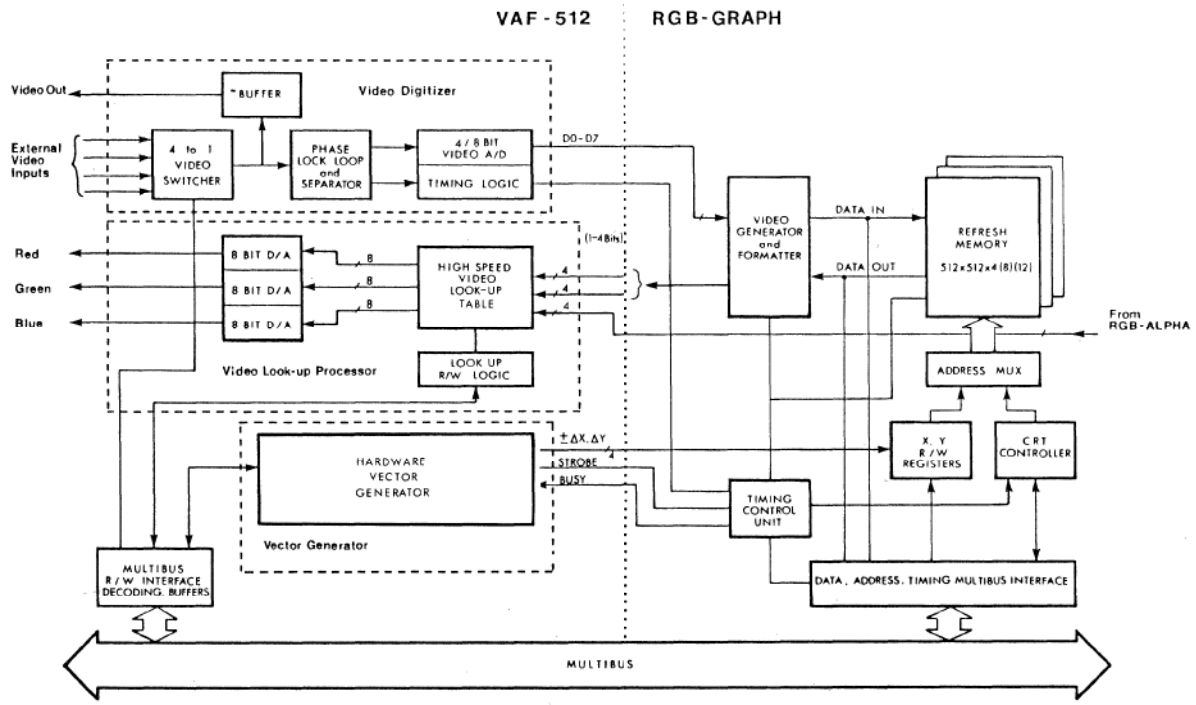


Figure 11. VAF-512 Video Processor

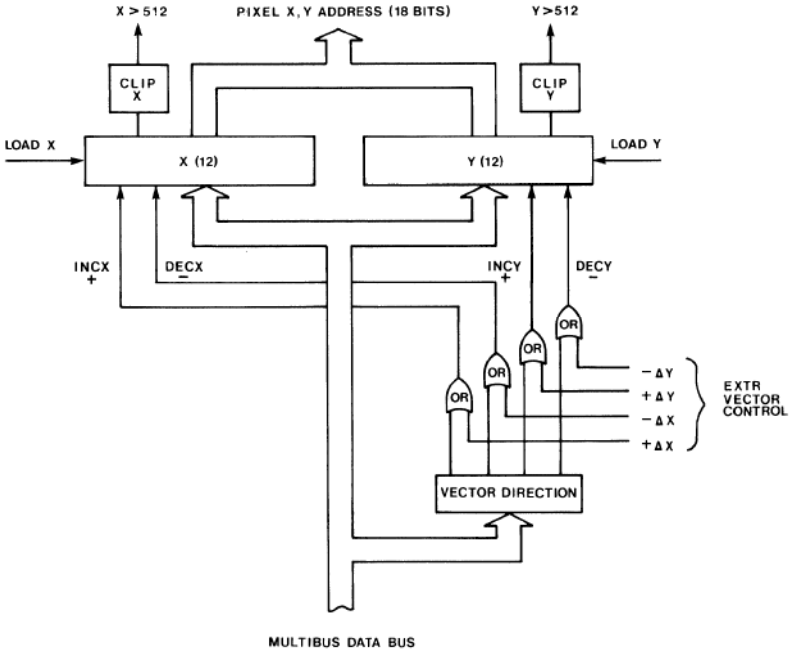


Figure 5. X,Y Registers

For high speed relative drawings, the vector plot feature can be used. By writing into the Vector Register the draw ing direction (4 bits), the X and Y Registers are automatically incremented/decremented (figure 6).

The vector plot can be interfaced with the hardware vector generator contained on the VAF-512 board. The VAF vector generator generates ± △X, ± △Y increment/decrement pulses when drawing vectors, circles, etc. at the speed of 800ns/pixel. The vector plot function can also be used for drawing pictures without tying up the system bus in multiprocessor applications by connecting the ± △X, ± △Y inputs to the I/O ports of the CPU board.

The X, Y Registers are also used in the DMA mode for autoincrementing the RAM address within the 1K byte DMA block.

The **Video Generator** performs three basic functions: conversion of digital data from the refresh RAM into the proper video signals to drive B/W and color monitors, conversion of digital video data from a frame grabber into a format required to write the data into the reresh RAM at video speeds, and the performance of various other video processing functions in hardware (zoom, scroll, overlay, clipping, video masking, doubling the horizontal resolution, etc.). The Video Generator is shown in figure 7.

Data is read from the display RAM as 4 consecutive pixels at one time for each plane (for refresh each plane looks like 512 rows x 128 strings/row x 4 1-bit pixels/string). This 4 pixel data is loaded into a shift register and then shifted out at the video clock speed (10MHz for 512 x 512 resolution) to produce a serial TTL signal for each plane (four in total).

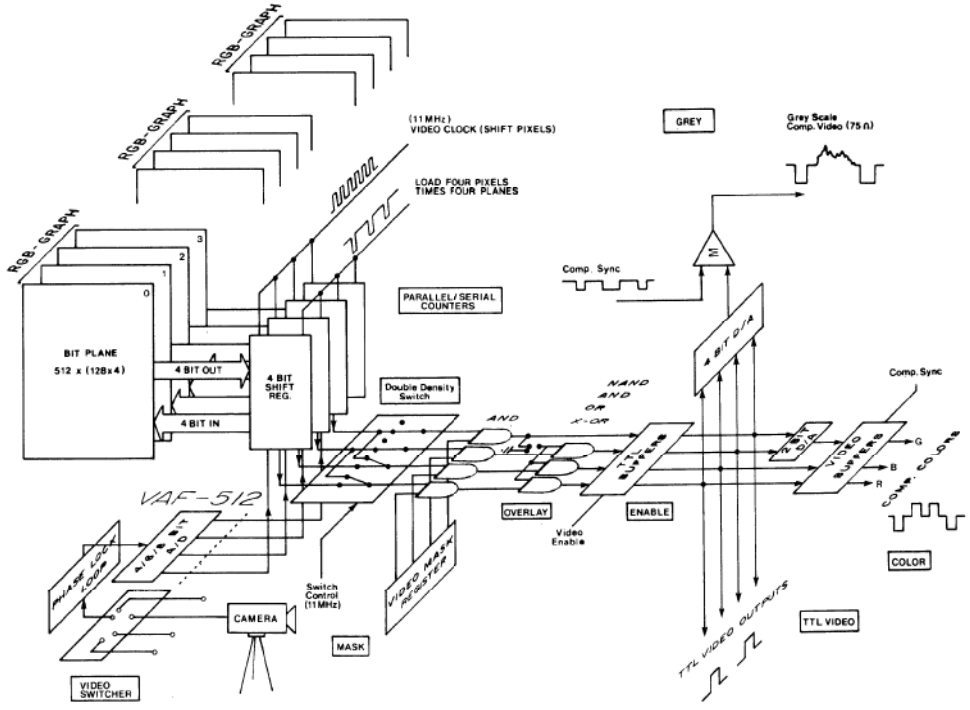


Figure 7. RGB-GRAPH Video Generator

SPECIFICATIONS

FUNCTIONAL

MEMORY ACCESS TIME

CRTC Data, CRTC Address, CRTC Status, and Vector Register access time is fixed at 500ns.
Access time to all other locations (including DMA) varies from 50ns to 1.2 μs for boards using 64K parts (see ORDERING INFORMATION), and from 50ns to 2.4 μs for boards using 16K parts. Average access time for 64K boards is approximately 800ns, and for 16K boards is about 1600ns.

DISPLAY PARAMETERS

RESOLUTION	RAM TYPE
256x 256 x 4	16K
512x 256 x 2	16K
512 x 512 x 4	64K
1024 x 512 x 2	64K

VIDEO TIMING

For a display format of 512 horizontal dots x 512 vertical dots on a monitor with a 51.2μs active video time a 10.000 MHz crystal is used. The following table gives the timing in both American and European standards.

SIGNAL	AMERICAN	EUROPEAN
Active Video	51.2 μs	51.2 μs
Horizontal Sync Frequency	15.82 KHz	15.82 KHz
Horizontal Sync Width	4.80 μs	4.80 μs
Vertical Sync Frequency	62.2 Hz	51.2 Hz
Vertical Sync Width	189.6 μs	189.6 μs

INPUT SIGNALS

Light-pen Enable
Lignt-pen Strobe

OUTPUT SIGNALS

TTL Level Video: TTL level Red
TTL level Green0
TTL level Green1
TTL level Blue
Vertical Drive
Horizontal Drive

Analog Video: Red
Green (composite)
Blue
Grey Scale (composite)

BUS INTERFACE

Address, data and control signals conform to Intel Multibus Specification No. 9800683
Command and Status Registers — Selectable on 16 byte I/O address boundaries 000 — FFF (0A0H)
Display Refresh Memory (DMA only) — Selectable on 1K byte memory address boundaries 0000-FFFFF (07C00H)

CONNECTORS

DESCRIPTION		MATING CONNECTOR
P1 : 86 pin edge connector, 0.156" centers,	Multibus interface	COMPAR ESM-43-DSRI
J1 : 10 pin right angle header,	Analog video outputs	AMP 87922-1
J2 : 10 pin right angle header,	TTL video outputs	AMP 87922-1
J3 : 50 pin right angle header,	Matrox video bus	Molex 15-25-4505
J4 : 10 pin right angle header,	Light pen interface	AMP 87922-1

PHYSICAL

SIZE

Width — 12.00 in. (30.48 cm)
Height — 6.75 in. (17.15cm)
Depth — 0.50 in. (1.27cm)

POWER REQUIREMENTS

64K — ±5V DC ±5% @ 2.25A
16K — ±5V DC ±5% @ 1.80A
+12V DC ±5% @ 128mA
−12V DC ±5% @ 30mA

ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 0%C to 55%C
Relative Humidity: 0° to 95° non-condensing

ORDERING INFORMATION

RGB-G/XX /X
- X — Number of bits per pixel (1/4)
- XX — Type of RAM (16/64)

Example: RGB-G/64/4: 512 x 512 color graphics controller with four bit planes

Note: The RGB-GRAPH should be ordered in exact configurations. User field upgrades (different resolutions, more bits/pixel) are not recommended as these require straps and PROM.

Software Support:
GRAS-80: CP/M compatible graphics primitives library